

Diodes as gatekeepers

Diode-resistor logic (DRL): the simplest gates you can build, and exactly why they are not enough.

01 COLD OPEN 0–5 min

Can two switches make a decision?

Your car beeps if **you are seated AND the belt is unfastened**, OR the door is open AND the key is in.

$$\text{Beep} = (\text{Seated} \cdot \overline{\text{Belt}}) + (\text{Door} \cdot \text{Key})$$

Somebody had to build that decision out of electricity. What is the cheapest part that can do it?



POP CULTURE

Minecraft players build working calculators from redstone "gates". Same idea: a gate is anything that turns input levels into an output level by a fixed rule. Today's gate-builder is the cheapest decision-maker in electronics: the diode.

THINK DEEPER

Before we start: which part of this beep rule do you think a handful of diodes *cannot* build?

Diodes can do the AND and the OR. They cannot do the **NOT** (the bar over Belt). That cliffhanger is next class.

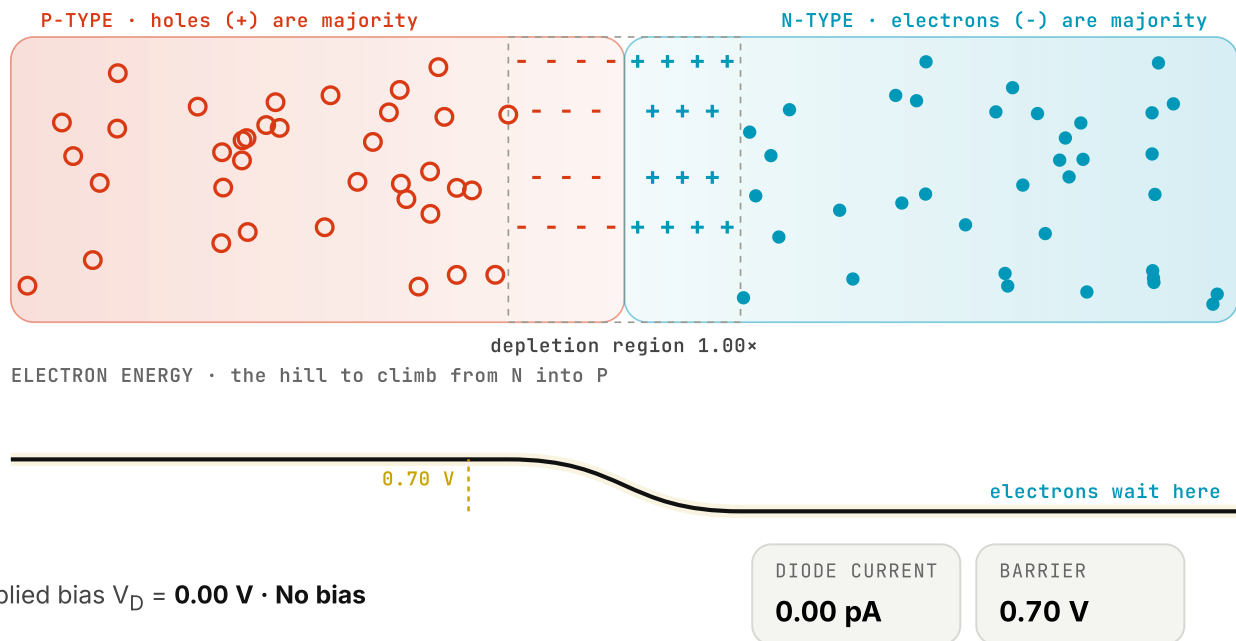
A STRONG ANSWER MENTIONS

- The overline: NOT. Diodes cannot invert.
- AND and OR are fine (today).
- That gap is why Week 1 Class 2 adds a transistor.

Inside the diode: a hill you can flatten

Inside the diode: the PN junction

Drag the bias. Watch the depletion region breathe and the barrier hill shrink.



The diode, four ways

Every diode analysis starts by choosing a model. The real curve is Shockley's equation. For logic we almost always use the **constant-drop** model.

$$I_D = I_S \left(e^{V_D/nV_T} - 1 \right), \quad V_T = \frac{kT}{q} \approx 25.9 \text{ mV}$$



GOTCHA

0.7 V is a model, not a law. Silicon turns on gradually around 0.6–0.7 V; germanium near 0.3 V; Schottky 0.2–0.4 V; LEDs 1.8–3.3 V depending on colour.

Diode model switcher

Pick a model, slide V_S . The dot is where the load line meets the diode curve.

$V_S = 2.00 \text{ V}$

Circuit: $V_S \rightarrow 470 \Omega \rightarrow \text{diode} \rightarrow \text{ground}$.

DIODE

ON

V_D

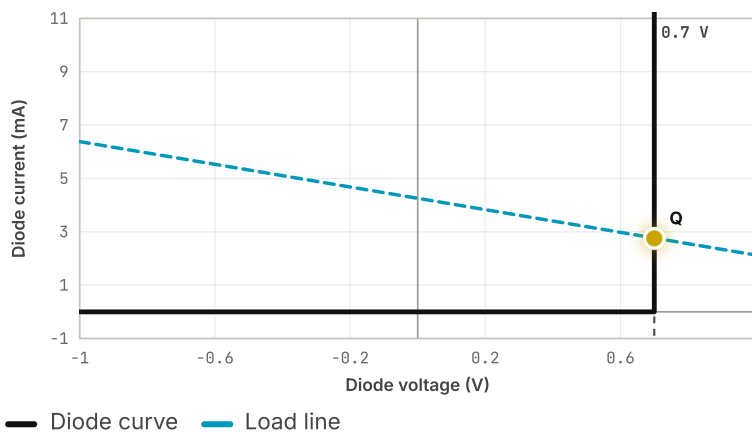
0.700 V

I_D

2.77 mA

V_R

1.30 V



04 CONCEPT 18-22 min

Agreeing on what a “1” is

Valid 1

$$V \geq V_{IH} = 2.0 \text{ V}$$

Forbidden zone

$0.8 \text{ V} < V < 2.0 \text{ V}$: the gate may read either, or oscillate

Valid 0

$$V \leq V_{IL} = 0.8 \text{ V}$$

A wire carries a **voltage**, not a bit. Logic families agree on bands. We use TTL-compatible thresholds all semester.

This is **positive logic**: higher voltage = 1. Negative logic flips the assignment, and the same circuit then performs the **dual** function.

THINK DEEPER

Why not make $V_{IL} = V_{IH} = 1.4 \text{ V}$ and get rid of the forbidden zone altogether?

A signal sitting near 1.4 V plus a few millivolts of noise would flicker between 0 and 1. The forbidden band is a **guard band**: a valid output is always far enough from the threshold that noise can't cross it.

A STRONG ANSWER MENTIONS

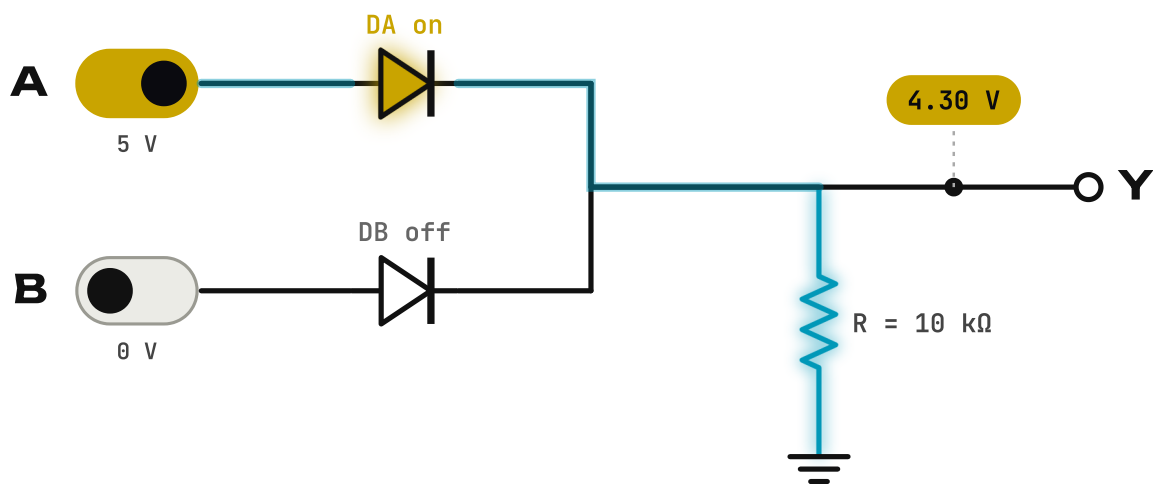
- Real signals carry noise; a single threshold turns small noise into random bit flips.
- Gates have finite gain; outputs cannot jump instantly at one exact voltage.
- The gap is what creates noise margin (Class 2).

05 **LIVE LAB** 22-28 min

Diode OR: the highest input wins

Diode OR gate Click the switches to flip inputs between 0 V and 5 V.

☐ Any input voltage V_Y 0.7 V (Si) ▼



OUTPUT
4.30 V

CURRENT IN R
0.430 mA

READS AS
Logic 1

BOOLEAN OR
1

Anodes at the inputs, cathodes joined, a resistor to ground.

Any 5 V input forward-biases its diode and lifts the output to

$$V_o = V_{max} - V_\gamma$$

Diodes on lower inputs are reverse-biased and drop out.



PRO TIP

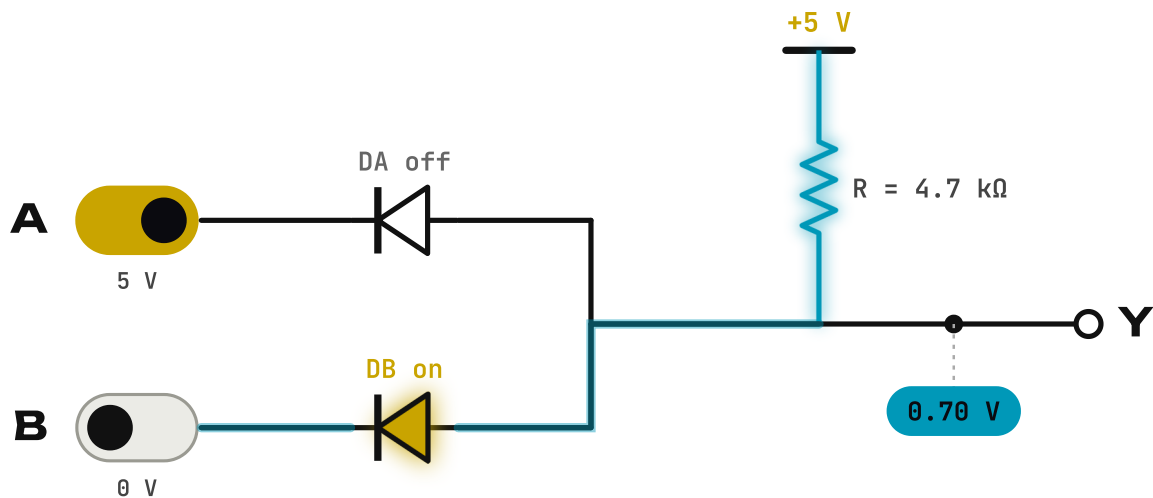
Find the input combination where **no** current flows at all.

06 **LIVE LAB** 28-33 min

Diode AND: the lowest input wins

Diode AND gate Click the switches to flip inputs between 0 V and 5 V.

☐ Any input voltage V_y 0.7 V (Si) ▼



OUTPUT
0.70 V

CURRENT IN R
0.915 mA

READS AS
Logic 0

BOOLEAN AND
0

Flip the diodes; move R to the supply. R pulls up, any 0 V input drags the node down to

$$V_o = V_{min} + V_\gamma$$



PRO TIP

Memory trick: the conducting diode is the one that **argues with the resistor**. R pulls down → highest input fights back (OR). R pulls up → lowest input fights back (AND).

Worked example: a diode AND gate

GIVEN

Two-input diode AND, $V_{CC} = 5\text{ V}$, $R = 4.7\text{ k}\Omega$, silicon diodes ($V_\gamma = 0.7\text{ V}$). Inputs $A = 0\text{ V}$, $B = 5\text{ V}$.

FIND

V_o , each diode's state, the current in R , and the logic level.

Method: assume-solve-verify, as in Boylestad Ch. 2 and Millman & Taub's diode-logic sections

SOLUTION

1. Guess which diode conducts. R pulls the joined anodes toward 5 V ; the diode whose cathode sits lowest forward-biases first: D_A (cathode at 0 V).

Diode circuits: assume states $\rightarrow$ solve $\rightarrow$ verify. If a check fails, change the assumption.

2. With D_A on it holds a fixed drop:

$$V_o = V_A + V_\gamma = 0 + 0.7 = 0.7\text{ V}$$

3. Verify D_B is off (anode at V_o , cathode at 5 V):

$$V_{D_B} = 0.7 - 5 = -4.3\text{ V} < V_\gamma \Rightarrow \text{OFF } \checkmark$$

4. All of R 's current flows through D_A into source A :

$$I_R = \frac{V_{CC} - V_o}{R} = \frac{5 - 0.7}{4.7\text{ k}\Omega} = 0.915\text{ mA}$$

5. $0.7\text{ V} \leq V_{IL} = 0.8\text{ V}$, so logic 0. $\text{AND}(0, 1) = 0\text{ } \checkmark$

Only 0.1 V separates this "0" from the forbidden zone. Hold that thought for the cascade.

ANSWER

$V_o = 0.7\text{ V}$ (logic 0). D_A ON, D_B OFF, $I_R = 0.915\text{ mA}$.

Worked example: three inputs, messy voltages

GIVEN

Three-input diode OR, $R = 10\text{ k}\Omega$, $V_\gamma = 0.7\text{ V}$. $A = 5\text{ V}$, $B = 3\text{ V}$, $C = 0\text{ V}$.

FIND

V_o , the diode states and I_R .

SOLUTION

1. OR gate: joined cathodes pulled down by R. The highest anode wins: D_A (5 V).

2. Output:

$$V_o = V_A - V_\gamma = 5 - 0.7 = 4.3 \text{ V}$$

3. Check the others (anode – cathode):

$$V_{D_B} = 3 - 4.3 = -1.3 \text{ V}, \quad V_{D_C} = 0 - 4.3 = -4.3 \text{ V} \Rightarrow \text{both OFF}$$

4. Current:

$$I_R = \frac{V_o}{R} = \frac{4.3}{10 \text{ k}\Omega} = 0.43 \text{ mA}$$

5. Twist: make B = 5 V too. D_A and D_B both conduct, V_o stays 4.3 V and matched diodes share 0.215 mA each.

Output depends only on the highest input. Extra 1s never push it higher.

ANSWER

$V_o = 4.3 \text{ V}$, only D_A conducts, $I_R = 0.43 \text{ mA}$.

09 **LIVE LAB** 44–50 min

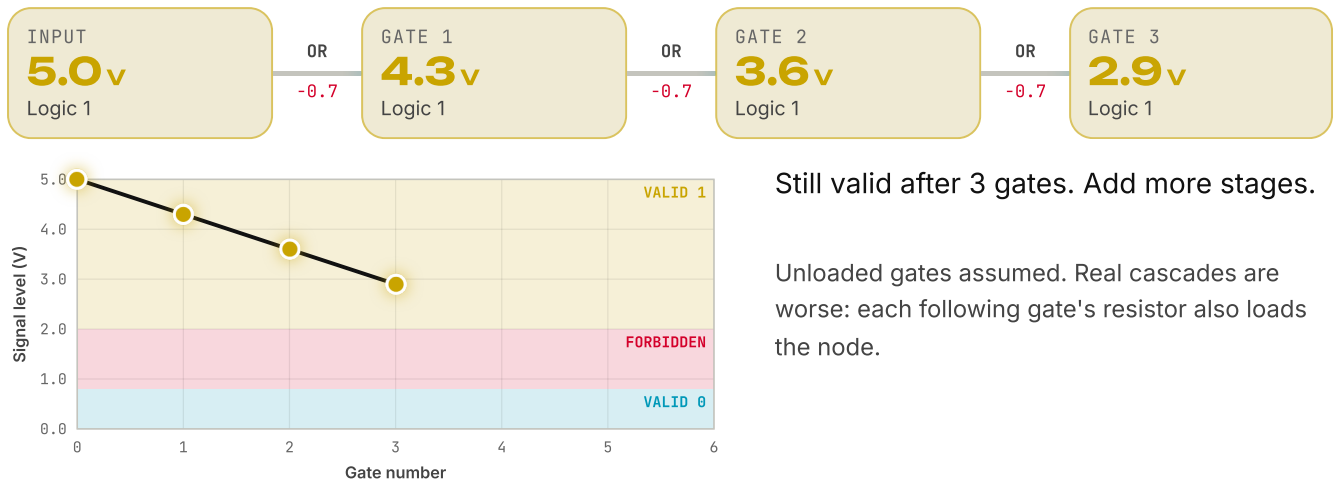
Why nobody builds a CPU from diodes

Three fatal flaws: **no inversion** (not functionally complete), **no power gain** (every stage weakens the signal), and a **V_γ tax** at every gate.

Cascade meltdown

Chain diode gates and watch a clean logic level walk into the forbidden zone.

Stages: 3



Still valid after 3 gates. Add more stages.

Unloaded gates assumed. Real cascades are worse: each following gate's resistor also loads the node.

10 YOUR TURN 50-55 min

Your turn • 1: a “zero” that isn’t

1 EXAM CQ

A three-input diode AND gate: $V_{CC} = 5\text{ V}$, $R = 10\text{ k}\Omega$, $V_Y = 0.7\text{ V}$.

Inputs: $A = 5\text{ V}$, $B = 5\text{ V}$, $C = 0.3\text{ V}$.

Find V_O , which diodes conduct, I_R , and the logic level.

SOLUTION

- Lowest input wins: D_C conducts.

$$V_O = 0.3 + 0.7 = 1.0\text{ V}$$

- Current in R :

$$I_R = \frac{5 - 1.0}{10\text{ k}\Omega} = 0.4\text{ mA}$$

- D_A, D_B : $1.0 - 5 = -4\text{ V} \rightarrow \text{OFF}$.

ANSWER

$V_O = 1.0\text{ V}$: in the forbidden zone. A 0.3 V “0” from a previous gate plus one diode drop is already unreadable.

Your turn • 2: the loading trap

2 TRAP

A diode OR gate ($R_1 = 10\text{ k}\Omega$ to ground) has **both inputs at 0 V**. Its output X feeds one input of a diode AND gate ($R_2 = 10\text{ k}\Omega$ to +5 V); the AND's other input is 5 V.

Find V_X . Is the OR gate's output still a 0?

SOLUTION

1. The OR diodes have anodes at 0 V: can they conduct? Only if the node is below -0.7 V . It isn't. Both OFF.
2. The AND gate's pull-up R_2 pushes current through the AND diode into node X, then down through R_1 . A voltage divider:

$$\frac{5 - 0.7 - V_x}{10\text{ k}} = \frac{V_x}{10\text{ k}}$$

3. Solve:

$$V_x = \frac{4.3}{2} = 2.15\text{ V}$$

ANSWER

The OR gate with both inputs at 0 V outputs **2.15 V: a logic 1**. The gates have corrupted each other. Fix: buffer with a transistor.

Critical thinking • design

a two-level diode circuit

3 DESIGN

Using only diodes and 10 k Ω resistors ($V_Y = 0.7$ V, $V_{CC} = 5$ V), build

$$Y = (A \cdot B) + C$$

Find Y for (A, B, C) = (5, 5, 0), (0, 0, 5) and (5, 0, 0) V. Does every output land in a valid band? How would you improve it?

SOLUTION

1. Structure: diode AND (A, B, R_A to +5 V) $\rightarrow$ node P $\rightarrow$ one input of a diode OR (with C) $\rightarrow$ Y, R_O to ground.
2. **Case A = B = 5 V, C = 0:** AND diodes off. Current flows +5 V $\rightarrow R_A \rightarrow$ P $\rightarrow$ OR diode $\rightarrow R_O \rightarrow$ ground:

$$\frac{5 - V_P}{10k} = \frac{V_P - 0.7}{10k} \Rightarrow V_P = 2.85 \text{ V}, Y = 2.15 \text{ V}$$

3. **Case A = B = 0, C = 5 V:** Y = 5 - 0.7 = 4.3 V. P = 0.7 V; the OR diode from P sees 0.7 - 4.3 < 0: off.
4. **Case A = 5 V, B = 0, C = 0:** P = 0.7 V, OR diode: anode 0.7 V with Y = 0 needs 0.7 V $\rightarrow$ on the edge, Y $\approx$ 0 V. Valid 0.

ANSWER

The logic is right but $Y = (A \cdot B) + C$ gives only 2.15 V for the A·B term: 0.15 V above V_{IH} . Two-level diode logic barely works, and a third level would fail. Improve it with $R_A \ll R_O$ (e.g. 1 k Ω / 10 k Ω $\rightarrow V_P = 4.61$ V, Y $\approx$ 3.9 V) at the cost of more current.

13 THINK DEEPER 65–68 min

Critical thinking • three

short arguments

THINK DEEPER

Input A comes from a sensor with $1\text{ k}\Omega$ internal resistance (open-circuit 5 V) into a diode OR with $R = 10\text{ k}\Omega$. Is the output still 4.3 V ?

No: the $1\text{ k}\Omega$ and $10\text{ k}\Omega$ divide the 4.3 V . $V_o \approx 3.91\text{ V}$. Still a 1, but the margin has shrunk by 0.4 V without any extra gate.

A STRONG ANSWER MENTIONS

- The source resistance forms a divider with R .
- $V_o = (5 - 0.7) \times 10 / (10 + 1) = 3.91\text{ V}$.
- Every real source has resistance; logic levels always sag under load.

THINK DEEPER

A classmate says: "Use germanium diodes ($V_y = 0.3\text{ V}$) and diode logic becomes cascable." Agree or disagree?

Partly. More stages survive (a 0 now dies at the third AND gate instead of the second), but the **fundamental** problems (no gain, no NOT, loading) are untouched. You have delayed the failure, not fixed it.

A STRONG ANSWER MENTIONS

- The loss per stage drops from 0.7 V to 0.3 V , so more stages survive.
- But there is still no gain and no inversion; loading still corrupts levels.
- Germanium also leaks more and is temperature sensitive.

14 REAL WORLD 68–72 min

Diode OR still ships everywhere: power ORing

Nobody builds logic from diodes today, but the diode OR lives inside every device that must never lose power. Feed a mains adapter and a battery to the load through two diodes: **whichever voltage is higher supplies the load**, and the other diode blocks backflow. No software, no switch, no delay.

At home: the IPS that keeps your fan running during load-shedding makes the same "whichever source is available" decision with relays and electronics.



BME CORNER

A bedside monitor or infusion pump cannot reboot when someone trips over the plug. Hospital equipment uses exactly this diode-OR, often with Schottky diodes or "ideal diode" MOSFET controllers to cut the 0.7 V loss. The same trick joins several bed call-buttons into one nurse-station lamp.

15 POP QUIZ 72-78 min

Pop quiz

1. A two-input diode OR gate ($V_Y = 0.7\text{ V}$) has inputs 0 V and 5 V. The output is:

- A. 5.0 V
- B. 4.3 V ✓
- C. 0.7 V
- D. 2.5 V

Highest input wins, minus one diode drop: $5 - 0.7 = 4.3\text{ V}$.

2. In a diode AND gate, which input sets the output?

- A. The highest
- B. The average
- C. The lowest ✓
- D. Only the supply

The lowest cathode forward-biases its diode and clamps the node at $V_{\min} + V_Y$.

3. Why can't diodes and resistors alone make a NOT gate?

- A. Diodes are too slow
- B. Passive networks cannot turn a high into a low: inversion needs gain ✓
- C. Resistors waste power
- D. They can, with enough diodes

A passive network's output always sits "between" its inputs. Inverting needs an active device: a transistor.

4. Under reverse bias, the depletion region...

- A. Disappears
- B. Gets wider and the barrier gets taller ✓
- C. Gets narrower
- D. Fills with free electrons

The applied voltage adds to the built-in potential: more uncovered ions, a wider region, a higher hill. Only a tiny leakage current flows.

5. A 5 V logic 1 passes through four cascaded diode OR gates. What arrives?

- A. 4.3 V
- B. 3.6 V
- C. 2.2 V ✓
- D. 1.5 V

$5 - 4 \times 0.7 = 2.2$ V. Barely above V_{IH} ; one more gate and it is lost.

16 RECAP 78-80 min

Three things to remember

O1

Diode OR: **highest** input wins, $V_{\max} - V_Y$. Diode AND: **lowest** input wins, $V_{\min} + V_Y$.

O2

Diode logic cannot invert, has no gain, loses 0.7 V per stage and loads its neighbours. It does not cascade.

O3

The fix is a transistor that restores levels and inverts. Next class: RTL, DTL, and a moon computer built from one gate.

HW

BEFORE NEXT CLASS

Diode OR, $R = 5 \text{ k}\Omega$, $V_Y = 0.6 \text{ V}$, inputs $A = 4 \text{ V}$, $B = 4.5 \text{ V}$. Find V_o , each diode's state and current. (Careful with D_A !)

SOLUTION

1. Highest input wins: D_B on.

$$V_o = 4.5 - 0.6 = 3.9 \text{ V}$$

2. D_A : $4 - 3.9 = 0.1 \text{ V} < 0.6 \text{ V} \rightarrow \text{OFF}$.

$$I_{D_B} = \frac{3.9}{5 \text{ k}} = 0.78 \text{ mA}, \quad I_{D_A} = 0$$

ANSWER

$V_o = 3.9 \text{ V}$, D_B on (0.78 mA), D_A off.

