

Adding a transistor: RTL to DTL

Give diode logic an inverter and it becomes a real, cascadable logic family.

01 COLD OPEN 0-5 min

The moon computer ran on one gate

The Apollo Guidance Computer (1969) was built from about 2,800 identical chips, each holding two 3-input **NOR** gates made of resistors and transistors.

One gate type. Every function. How?



POP CULTURE

The Lego approach: one brick shape, stacked cleverly, builds the whole Millennium Falcon. NOR is a brick that can build *any* logic function. Last class's diodes could not even make a NOT.

THINK DEEPER

Draw a NOT gate using only one 2-input NOR. Then an OR.

$\overline{A + A} = \overline{A}$, and $A + B = \overline{\overline{A + B}}$: a NOR followed by a NOR-inverter.

A STRONG ANSWER MENTIONS

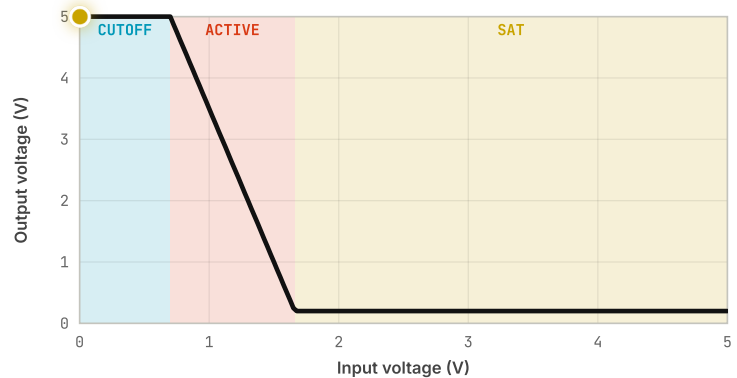
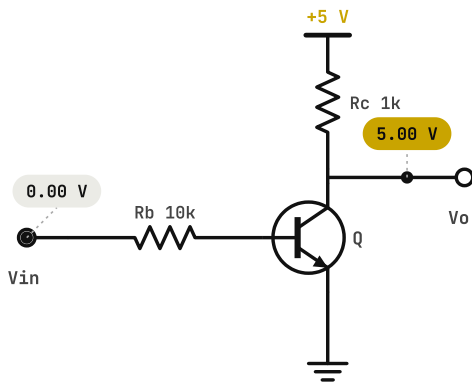
- NOT: tie both inputs together: $\text{NOR}(A, A) = \overline{A}$.
- OR: NOR followed by a NOR-as-NOT.
- One qualified part type = one thing to test for spaceflight.

02 LIVE LAB 5-15 min

The transistor as a switch

(60-second refresher)

Transistor inverter Slide the input. A good switch lives in cutoff or saturation and dashes through the middle.



$V_{in} = 0.00 \text{ V}$

$\beta (h_{FE}) = 50$

$R_B = 10 \text{ k}\Omega$

Cutoff · switch open

$$I_B = 0.000 \text{ mA} \cdot I_C = 0.00 \text{ mA}$$

CUTOFF

$V_{BE} < 0.5 \text{ V}$. $I_B \approx I_C \approx 0$. Switch open, output high.

ACTIVE

$I_C = \beta I_B$. Great for amplifiers, bad for logic.

SATURATION

$V_{CE(sat)} \approx 0.2 \text{ V}$. Needs $I_B \geq I_{C(sat)} / \beta_{min}$.

03 WORKED EXAMPLE 15-21 min

Worked example: design the inverter

GIVEN

$V_{CC} = 5 \text{ V}$, $R_C = 1 \text{ k}\Omega$, $R_B = 10 \text{ k}\Omega$, $\beta_{min} = 50$, $V_{BE} = 0.7 \text{ V}$, $V_{CE(sat)} = 0.2 \text{ V}$.

FIND

The minimum input voltage that saturates the transistor, and the overdrive factor at $V_{in} = 5 \text{ V}$.

Method: Millman & Taub, transistor switch; Boylestad, BJT switching networks

SOLUTION

1. A switch must reach saturation. Saturated collector current is set by R_C , not β :

$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{5 - 0.2}{1 \text{ k}\Omega} = 4.8 \text{ mA}$$

2. Minimum base current (design for the **worst** transistor: β_{min}):

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{min}} = \frac{4.8}{50} = 0.096 \text{ mA}$$

3. Input voltage that supplies it through R_B :

$$V_{in(min)} = V_{BE} + I_{B(min)} R_B = 0.7 + 0.096 \times 10 = 1.66 \text{ V}$$

4. Every valid 1 ($\geq 2.0 \text{ V}$) saturates the switch. At $V_{in} = 5 \text{ V}$:

$$I_B = \frac{5 - 0.7}{10 \text{ k}} = 0.43 \text{ mA}, \quad \text{overdrive} = \frac{0.43}{0.096} \approx 4.5$$

Designers overdrive 2–5× so temperature and β spread cannot pull the switch out of saturation. The price: extra stored charge and slower turn-off (next week).

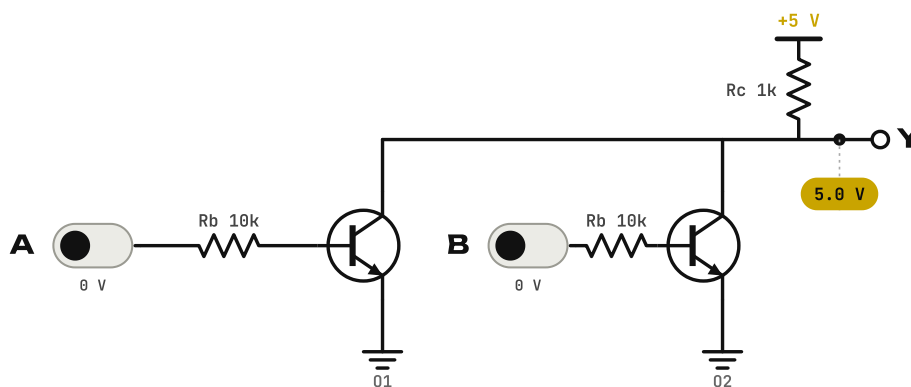
ANSWER

$V_{in(min)} = 1.66 \text{ V}$; at 5 V input the base is overdriven $\approx 4.5\times$.

04 LIVE LAB 21–26 min

RTL: one transistor per input

RTL NOR: the Apollo gate Either input high saturates its transistor and pulls the shared collector low.



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

I_B (HIGH INPUT)
0.43 mA

I_C
0.0 mA

$$Y = \overline{A + B}$$

Any high input saturates its own transistor and drags the **shared** collector low: NOR, the Apollo gate.

**GOTCHA**

RTL's weak spot: an input only needs $\approx 0.5\text{--}0.7\text{ V}$ to start turning on, and a real "0" is already 0.2 V . Tiny low noise margin. DTL raises that threshold.

05 **CONCEPT** 26–30 min

DTL NAND = diode AND + transistor NOT

Take last class's diode AND. Instead of using its output directly, feed it through two **level-shifting diodes** into a transistor inverter.

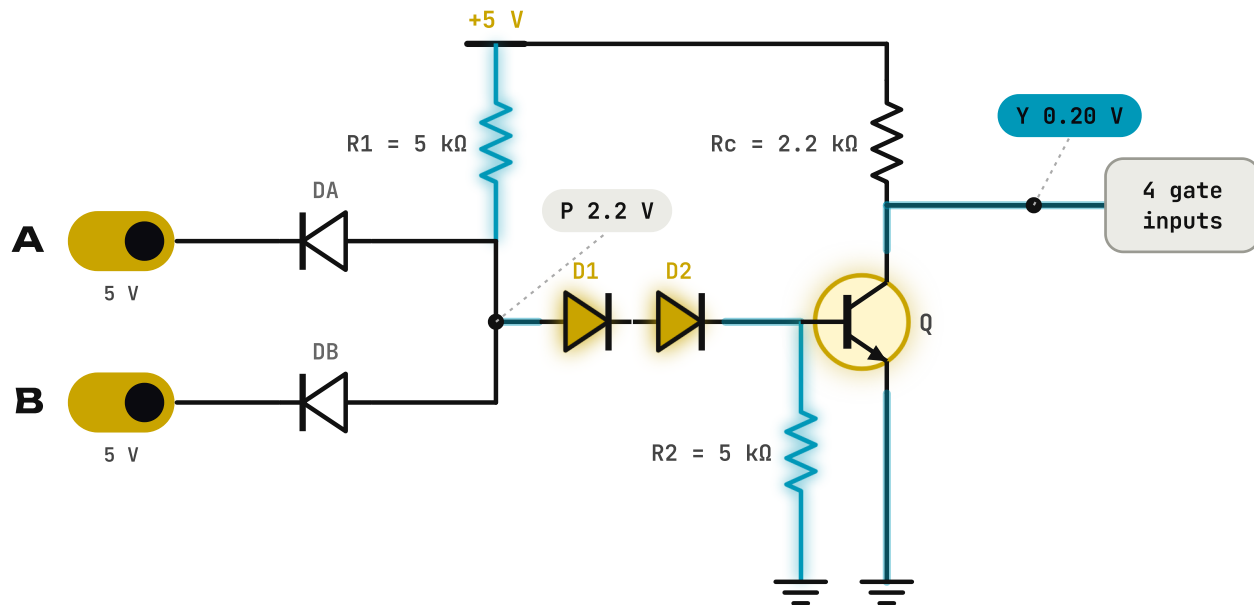
**PRO TIP**

Every part has one job. Exam CQs love "state the function of D_1 , D_2 and R_2 ".

R_1 + input diodes	The diode AND. Any low input steals R_1 's current.
D_1, D_2	Level shifters: each adds 0.7 V to what P needs to turn the transistor on $\rightarrow$ higher threshold, bigger noise margin.
R_2	Drains stored base charge so the transistor turns off fast; stops the base floating.
Transistor + R_C	The inverter: restores clean $0.2\text{ V} / 5\text{ V}$ and drives the next gates.

DTL NAND, live

DTL NAND gate Flip A and B. Then pile on fan-out and lower β until the output low breaks.



Fan-out $N = 4$

$\beta_{\min} = 30$

I1 THROUGH R1
0.56 mA

I R2
0.16 mA

I B
0.40 mA

MUST SINK
5.46 mA

B · IB AVAILABLE
12.00 mA

MAX FAN-OUT
11

Y = 0.

Both inputs high, the transistor saturates with $2.2\times$ the base drive it needs.

Worked example: analyse the DTL NAND

GIVEN

$V_{CC} = 5\text{ V}$, $R_1 = R_2 = 5\text{ k}\Omega$, $R_C = 2.2\text{ k}\Omega$, $V_Y = 0.7\text{ V}$, $V_{BE(\text{sat})} = 0.8\text{ V}$, $V_{CE(\text{sat})} = 0.2\text{ V}$, $V_{BE(\text{cut-in})} = 0.5\text{ V}$, $\beta_{\min} = 30$. Logic levels $0.2\text{ V} / 5\text{ V}$.

FIND

The output for (a) any input low and (b) all inputs high; check saturation.

SOLUTION

1. **Any input low (0.2 V):** that input diode conducts and clamps node P:

$$V_P = 0.2 + 0.7 = 0.9 \text{ V}$$

2. To push current into the base, P must reach two diode drops plus the base cut-in:

$$V_P \geq 0.7 + 0.7 + 0.5 = 1.9 \text{ V}$$

0.9 V < 1.9 V → transistor cut off → Y = 5 V. The current $(5 - 0.9)/5k = 0.82 \text{ mA}$ flows out through the low input.

3. **All inputs high (5 V):** input diodes reverse-biased; R_1 's current goes through D_1, D_2 into the base. Assume saturation:

$$V_P = V_{BE(sat)} + 2V_\gamma = 0.8 + 1.4 = 2.2 \text{ V}$$

4. Currents at node P and the base:

$$I_1 = \frac{5-2.2}{5k} = 0.56, \quad I_{R2} = \frac{0.8}{5k} = 0.16, \quad I_B = 0.40 \text{ mA}$$

5. Collector current (no load) and the saturation check:

$$I_C = \frac{5-0.2}{2.2k} = 2.18 \text{ mA} < \beta_{min} I_B = 30 \times 0.40 = 12.0 \text{ mA} \checkmark$$

6. Input diodes: anode 2.2 V, cathode 5 V → -2.8 V, off ✓. Y = 0.2 V.

Y is 0 only when A AND B are 1: NAND.

ANSWER

Any input low → Q off, Y = 5 V. All high → $I_B = 0.40 \text{ mA}$, saturated, Y = 0.2 V.

08 WORKED EXAMPLE 43-48 min

Worked example: how many gates can it drive?

GIVEN

The same gate, output low (Y = 0.2 V), driving N identical DTL gates.

FIND

Maximum fan-out N.

**GOTCHA**

Fan-out is decided in the **low** output state. When Y is high the driven gates' input diodes are reverse-biased and draw almost nothing.

SOLUTION

- Each driven gate has a **low** input (our $Y = 0.2$ V), so each one dumps its R_1 current into our collector:

$$I_L = \frac{V_{CC} - (V_{CE(sat)} + V_\gamma)}{R_1} = \frac{5 - 0.9}{5 \text{ k}} = 0.82 \text{ mA}$$

- Total collector current with N loads:

$$I_C = 2.18 + 0.82N \text{ mA}$$

- Stay saturated: $I_C \leq \beta_{\min} I_B$:

$$2.18 + 0.82N \leq 12.0 \Rightarrow N \leq 11.97$$

- Round **down**: a fraction of a gate is no gate.

$$N_{\max} = 11$$

Try it: set $\beta = 30$, $N = 12$ in the DTL lab and watch Y leave the valid-0 band.

ANSWER

Fan-out = 11 (with $\beta_{\min} = 30$).

09 **CONCEPT** 48-52 min

Noise margin: why two level-shift diodes?

Noise margin = how much garbage a signal can pick up and still be read correctly. Low state: the input must stay below the voltage that starts turning the transistor on.

$$V_{th} = V_{P,on} - V_\gamma = 1.9 - 0.7 = 1.2 \text{ V}, \quad NM_L = 1.2 - 0.2 = 1.0 \text{ V}$$

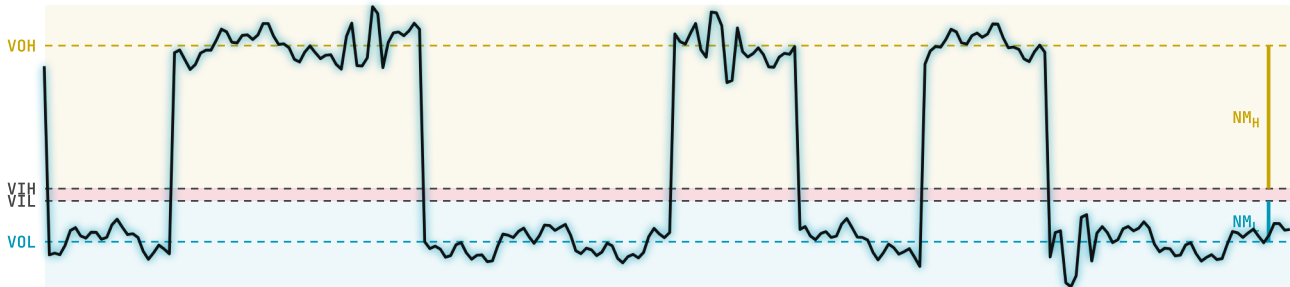
High state, roughly: input diodes stay off while $V_{in} > V_P - V_\gamma = 1.5$ V, so $NM_H \approx 5 - 1.5 = 3.5$ V (unloaded).

LEVEL-SHIFT DIODES	V_P TO TURN ON	INPUT THRESHOLD	NM_L
0 (just the base)	0.5 V	≈ -0.2 V (fails!)	none
1	1.2 V	0.5 V	0.3 V
2 (course DTL)	1.9 V	1.2 V	1.0 V

See a noise margin fail

Noise-margin scope Turn up the noise. Red ticks = the receiver read the wrong bit (or couldn't decide).

Noise amplitude $\pm 0.60\text{ V}$ (peak $\approx 1.2\text{ V}$)



receiver errors ▲

NM LOW

1.00 V

NM HIGH

3.50 V

SAMPLES MISREAD

0 %

Errors start when the noise peak exceeds the **smaller** margin. A family is only as robust as its weaker side.

Your turn • 1: cheap transistors

1

EXAM CQ

In the course DTL NAND, replace the transistor with one whose $\beta_{\min} = 20$. Everything else is unchanged.

What is the new fan-out?

SOLUTION

1. Available collector current:

$$\beta_{\min} I_B = 20 \times 0.40 = 8.0\text{ mA}$$

2. Fan-out condition:

$$2.18 + 0.82N \leq 8.0 \Rightarrow N \leq 7.1$$

ANSWER

N = 7. Cheaper transistors (lower β) directly cost fan-out.

Your turn • 2: a bigger R_2

2 EXAM CQ

Change R_2 to $10\text{ k}\Omega$ ($\beta_{\min} = 30$). Find I_B and the fan-out.

What do you lose?

SOLUTION

1. New R_2 current and base current:

$$I_{R2} = \frac{0.8}{10\text{k}} = 0.08\text{ mA}, \quad I_B = 0.56 - 0.08 = 0.48\text{ mA}$$

2. Fan-out:

$$30 \times 0.48 = 14.4 \Rightarrow N \leq \frac{14.4 - 2.18}{0.82} = 14.9 \Rightarrow N = 14$$

ANSWER

Fan-out rises to 14, but stored base charge now drains through a larger resistor: **slower turn-off**. Speed versus drive is the eternal trade.

Your turn • 3: spot the wrong claim

3 TRAP

A classmate says: "Fan-out is limited when the output is high, because the output must supply current to all the loads."

Is that right for DTL? Explain which state limits fan-out and why.

SOLUTION

ANSWER

Wrong for DTL. In the high state the driven inputs' diodes are reverse-biased and draw only leakage. The limit comes from the **low** state, where each load pushes $\approx 0.82\text{ mA}$ into the saturated collector.

Critical thinking • design for fan-out 10

4 DESIGN

A customer needs the course DTL gate to drive **10 loads** with $\beta_{\min} = 30$. You may change only R_C .

What is the smallest R_C that works? Pick a standard value and state the trade-off.

SOLUTION

- Budget for the collector at $\beta_{\min} = 30$:

$$\beta_{\min} I_B = 12.0 \text{ mA} \geq I_{RC} + 10 \times 0.82$$

- So the pull-up may take at most

$$I_{RC} \leq 12.0 - 8.2 = 3.8 \text{ mA} \Rightarrow R_C \geq \frac{4.8}{3.8} = 1.26 \text{ k}\Omega$$

- Choose a standard value with margin: **1.5 k Ω** ($I_{RC} = 3.2 \text{ mA} \rightarrow N \leq 10.7$).

Bigger R_C helps fan-out but slows the low-to-high edge: the output charges load capacitance through R_C . TTL's totem-pole fixes exactly this (Week 3).

ANSWER

$R_C \geq 1.26 \text{ k}\Omega$; pick 1.5 k Ω . Too large and the rising edge gets slow.

Critical thinking • then why

not five level shifters?

5

CRITICAL THINKING

Two level-shift diodes gave $NM_L = 1.0$ V. A student proposes **five** diodes for an even bigger margin.

Analyse $n = 3, 4, 5$ (all else as the course DTL, $\beta_{\min} = 30$). What goes wrong?

SOLUTION

1. With n level-shift diodes, $V_{P(on)} = 0.8 + 0.7n$ and $I_1 = (5 - V_P)/5 \text{ k}\Omega$, $I_{R2} = 0.16 \text{ mA}$:
2. **$n = 3$:** $V_P = 2.9 \text{ V}$, $I_B = 0.42 - 0.16 = 0.26 \text{ mA} \rightarrow$ fan-out $(7.8 - 2.18)/0.82 = 6.9 \rightarrow 6$. NM_L rises to $\approx 1.7 \text{ V}$ but the high-side threshold rises to 2.2 V , so NM_H falls to $\approx 2.8 \text{ V}$.
3. **$n = 4$:** $I_B = 0.12 \text{ mA} \rightarrow$ fan-out 1.
4. **$n = 5$:** $V_P = 4.3 \text{ V}$, $I_1 = 0.14 \text{ mA} < I_{R2} = 0.16 \text{ mA} \rightarrow I_B < 0$.

The transistor can never saturate: the gate is dead.

ANSWER

Each extra diode buys low-side margin but steals base drive and high-side margin. Two is the sweet spot for a 5 V supply.

16 REAL WORLD 71-74 min

Fan-out lives on in every board you build

An Arduino or Raspberry Pi pin has a current limit, exactly like our DTL collector. Hang too many LEDs or chip inputs on one pin and the "low" stops being low, or the pin is damaged. Datasheets still list the I_{OL}/I_{IL} currents fan-out is computed from (TTL version in Week 3).



BME CORNER

In a patient monitor one sensor signal may feed an ADC, a display driver and an alarm comparator at once. Every extra input loads the source and the reading drifts. The fix is DTL's idea: a buffer stage, so the fragile source drives only one input. The op-amp version (voltage follower) comes in Week 8.

17 POP QUIZ 74-78 min

Pop quiz

1. In a BJT switch, the saturated collector current is set mainly by:

- A. β
- B. R_B
- C. V_{CC} and R_C ✓
- D. The input frequency

In saturation the transistor is a closed switch: $I_{C(sat)} = (V_{CC} - V_{CE(sat)})/R_C$. β only decides whether you get there.

2. Why design with β_{min} , not typical β ?

- A. Bigger numbers
- B. It must work for the worst transistor in the batch and at low temperature ✓
- C. Datasheets only list β_{min}
- D. β never varies

β spreads widely between parts and falls with temperature. Design for the worst case.

3. An RTL gate with one transistor per input and a shared R_C is a...

- A. NAND
- B. NOR ✓
- C. AND
- D. XOR

Any high input saturates its transistor and pulls the shared output low: NOT(A + B).

4. What limits DTL fan-out?

- A. Current from each driven input flowing into the saturated collector (low state) ✓
- B. Diode drops at the inputs
- C. The speed of R_2
- D. The number of input diodes

Each low-driven input sinks ≈ 0.82 mA into the driver. Too many and $\beta_{min}I_B$ cannot hold saturation.

5. A family has $NM_L = 1.0$ V and $NM_H = 3.5$ V. The largest noise it tolerates on every signal is:

- A. 4.5 V
- B. 3.5 V
- C. 2.25 V
- D. 1.0 V ✓

A chain is as strong as its weakest link: the smaller margin decides.

18 **RECAP** 78-80 min

Three things to remember

01

A logic transistor lives in cutoff or saturation. Saturation needs $I_B \geq I_{C(sat)}/\beta_{min}$.

02

DTL = diode AND + level-shift diodes + transistor NOT = NAND. Level shifters buy noise margin; R_2 buys speed.

03

Fan-out is set in the low state: $2.18 + 0.82N \leq \beta_{\min} I_B$. Next week: switching speed and MOSFET gates.

HW

BEFORE NEXT CLASS

Same DTL gate but $R_C = 4.7 \text{ k}\Omega$ ($\beta_{\min} = 30$). Find the fan-out. Does a bigger R_C help or hurt when driving capacitive loads?

SOLUTION

1. New pull-up current:

$$I_{RC} = \frac{4.8}{4.7 \text{ k}} = 1.02 \text{ mA}$$

2. Fan-out:

$$N \leq \frac{12.0 - 1.02}{0.82} = 13.4 \Rightarrow 13$$

ANSWER

Fan-out 13, but the rising edge is $\approx 2\times$ slower ($4.7 \text{ k}\Omega$ vs $2.2 \text{ k}\Omega$ charging the load capacitance): exactly what TTL's totem-pole fixes.

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