

MOSFET switches and MOS gates

A switch you drive with voltage instead of current, and the NMOS inverters, NANDs and NORs built from it.

01 **COLD OPEN** 0–4 min

15 billion switches, and your phone isn't on fire

A current flagship phone chip holds roughly **15–20 billion** transistors.



POP CULTURE

Doctor Strange checked 14,000,605 futures. Your phone's processor has about a thousand times more switches than that, and each one flips up to a few billion times per second.

Last class the BJT switch needed base current just to stay on. Multiply that by 15 billion.

THINK DEEPER

Suppose every one of 15 billion switches leaked just $1\ \mu\text{A}$ from a 1 V supply while idle. How much power is that?

15 kW, in your pocket. The phone battery would last under a second. Real chips idle at milliwatts, so each switch must leak far less than a nanoamp. Today we meet the switch that makes that possible, and the first logic built from it, which *did* burn power.

A STRONG ANSWER MENTIONS

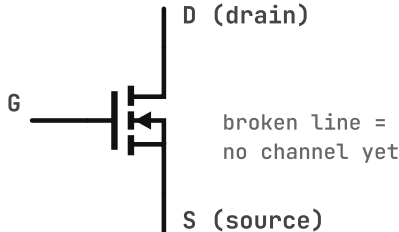
- $15 \times 10^9 \times 1\ \mu\text{A} = 15\ 000\ \text{A}$.
- $P = 1\ \text{V} \times 15\ 000\ \text{A} = 15\ \text{kW}$: about seven 2 kW electric kettles.
- So a modern chip must draw almost zero current when it is not switching.

02 **CONCEPT** 4–9 min

Enhancement NMOS: the gate builds its own wire

- **Structure:** p-type substrate, two heavily doped n^+ islands (source S, drain D), a thin SiO_2 insulator and a gate G on top. *Metal–Oxide–Semiconductor*.

- $V_{GS} = 0$: S and D are two back-to-back pn junctions. No path, no current. **Normally OFF** (enhancement mode).
- $V_{GS} > V_T$: positive gate charge pulls electrons to the surface and **inverts** it into a thin n-channel joining S to D. V_T is the *threshold voltage* ($\approx 0.3\text{--}1\text{ V}$ on chips, $1\text{--}4\text{ V}$ in power MOSFETs).
- The gate is a capacitor plate:** in DC, $I_G \approx 0$. The input is controlled by voltage, not current.



★

POP CULTURE

The channel is Hogwarts' Room of Requirement: it doesn't exist until you ask hard enough ($V_{GS} > V_T$), and the harder you ask, the bigger it gets.

03 **LIVE LAB** 9–16 min

Grow a channel, then pinch it off

NMOS explorer: build a channel, then pinch it

Raise V_{GS} past V_T to grow the channel; raise V_{DS} past $V_{GS} - V_T$ to pinch it off at the drain.

$V_{GS} = 3.00\text{ V}$
 $V_{DS} = 4.00\text{ V}$

$V_T = 1.00\text{ V}$
 $k = 0.50\text{ mA/V}^2$

REGION

Saturation · current source

I_D
2.00 mA

$V_{GS} - V_T$
2.00 V

$R_{DS(ON)} \approx 1/[2K(V_{GS}-V_T)]$
500 Ω

04 **CONCEPT** 16–21 min

Three regions, three equations

REGION	CONDITION	DRAIN CURRENT
Cutoff	$V_{GS} < V_T$	$I_D = 0$
Triode	$V_{DS} < V_{GS} - V_T$	$I_D = k \left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2 \right]$

REGION	CONDITION	DRAIN CURRENT
Saturation	$V_{DS} \geq V_{GS} - V_T$	$I_D = k(V_{GS} - V_T)^2$

For a small V_{DS} drop the V_{DS}^2 term: the channel is a **voltage-controlled resistor**.

$$I_D \approx 2k(V_{GS} - V_T) V_{DS} \Rightarrow r_{DS(on)} \approx \frac{1}{2k(V_{GS} - V_T)}$$

Cutoff

open switch

Triode

closed switch, $r_{DS(on)}$

Saturation

current source: only passed through while switching



GOTCHA

Name trap. A *saturated BJT* is a closed switch. A *saturated MOSFET* is a current source (like BJT active). The MOSFET's closed-switch region is **triode**.

05 WORKED EXAMPLE 21-27 min

Worked example: region and current

GIVEN

Enhancement NMOS with $k = 0.4 \text{ mA/V}^2$, $V_T = 1.5 \text{ V}$.

FIND

Region and I_D for (a) $V_{GS} = 1 \text{ V}$, $V_{DS} = 5 \text{ V}$; (b) $V_{GS} = 4 \text{ V}$, $V_{DS} = 5 \text{ V}$; (c) $V_{GS} = 4 \text{ V}$, $V_{DS} = 0.5 \text{ V}$.
(d) $r_{DS(on)}$ at $V_{GS} = 4 \text{ V}$; compare with V_{DS}/I_D in (c).

Method: compute the overdrive, compare with V_{DS} , then pick the equation (Boylestad, enhancement MOSFET analysis)

SOLUTION

1. **(a)** $V_{GS} = 1 \text{ V} < V_T = 1.5 \text{ V}$: no channel $\rightarrow$ **cutoff**, $I_D = 0$.

2. **(b)** Overdrive first: $V_{GS} - V_T = 2.5 \text{ V}$. $V_{DS} = 5 \text{ V} \geq 2.5 \text{ V} \rightarrow$ **saturation**:

$$I_D = k(V_{GS} - V_T)^2 = 0.4(2.5)^2 = 2.5 \text{ mA}$$

Always compute the overdrive and compare it with V_{DS} before choosing an equation.

3. **(c)** $V_{DS} = 0.5 \text{ V} < 2.5 \text{ V} \rightarrow$ **triode**:

$$I_D = 0.4 [2(2.5)(0.5) - 0.5^2] = 0.4(2.25) = 0.9 \text{ mA}$$

4. (d) On-resistance vs the actual ratio at (c):

$$r_{DS(on)} \approx \frac{1}{2(0.4)(2.5)} = 0.5 \text{ k}\Omega, \quad \frac{V_{DS}}{I_D} = \frac{0.5 \text{ V}}{0.9 \text{ mA}} = 556 \Omega$$

About 11 % higher: the $-V_{DS}^2$ term. The resistor model is best when $V_{DS} \ll V_{GS} - V_T$.

ANSWER

(a) cutoff, 0 · (b) saturation, 2.5 mA · (c) triode, 0.9 mA · (d) $r_{DS(on)} \approx 500 \Omega$ (556 Ω actual at 0.5 V).

06 CONCEPT 27–30 min

Why MOSFETs won the switch war

	BJT SWITCH (LAST CLASS)	MOSFET SWITCH
Controlled by	base current I_B	gate voltage V_{GS}
DC input current when ON	$I_B \geq I_{C(sat)}/\beta$, all the time	≈ 0 (insulated gate)
ON voltage	$V_{CE(sat)} \approx 0.2 \text{ V}$, fixed	$I_D \cdot r_{DS(on)}$, can be millivolts
Turn-off delay	storage time t_s : excess minority charge	no storage time (majority carriers)
The catch	—	gate capacitance must be charged and discharged every switch



GOTCHA

Zero DC gate current is **not** zero gate current. The gate is a capacitor: each transition needs a charge $Q = C_G \cdot \Delta V$ delivered in a short time, which means a large transient current.

Remember t_s from last class, the BJT that refused to switch off? A MOSFET has nothing stored in a base to sweep out; its speed is set only by how fast you can move gate charge.

07 THINK DEEPER 30–33 min

Critical thinking • “zero gate

current”, so why a gate driver?



CRITICAL THINKING

A drone's motor controller uses a power MOSFET: total gate charge $Q_g = 60 \text{ nC}$ (at $V_{GS} = 10 \text{ V}$), $V_{GS(th)} = 2\text{--}4 \text{ V}$, switched by **20 kHz PWM**.

A student connects it straight to a 3.3 V microcontroller pin (20 mA max): "MOSFETs draw no gate current, so it's fine."

Explain, with numbers, why the MOSFET gets hot and why engineers add a **gate driver**.

SOLUTION

1. Charging time with the pin's 20 mA (even pretending 3.3 V were enough):

$$t \approx \frac{Q_g}{I} = \frac{60 \text{ nC}}{20 \text{ mA}} = 3 \mu\text{s}$$

2. At 20 kHz the PWM period is 50 μs with two transitions: about 6 μs , $\approx 12\%$ of every cycle, spent half-on in saturation where V_{DS} and I_D are both large $\rightarrow$ switching loss, heat.
3. Worse: $V_{GS(th)}$ can be up to 4 V. A 3.3 V pin may not turn it on at all, and $r_{DS(on)}$ is only guaranteed at $V_{GS} = 10 \text{ V}$.
4. A gate driver supplies 10–12 V and amps of peak current:

$$t \approx \frac{60 \text{ nC}}{2 \text{ A}} = 30 \text{ ns} \quad (100 \times \text{faster})$$

ANSWER

The gate needs no *DC* current but lots of *transient* charge, and enough *voltage*. A driver delivers both: 30 ns edges at 10 V instead of 3 μs edges at 3.3 V.

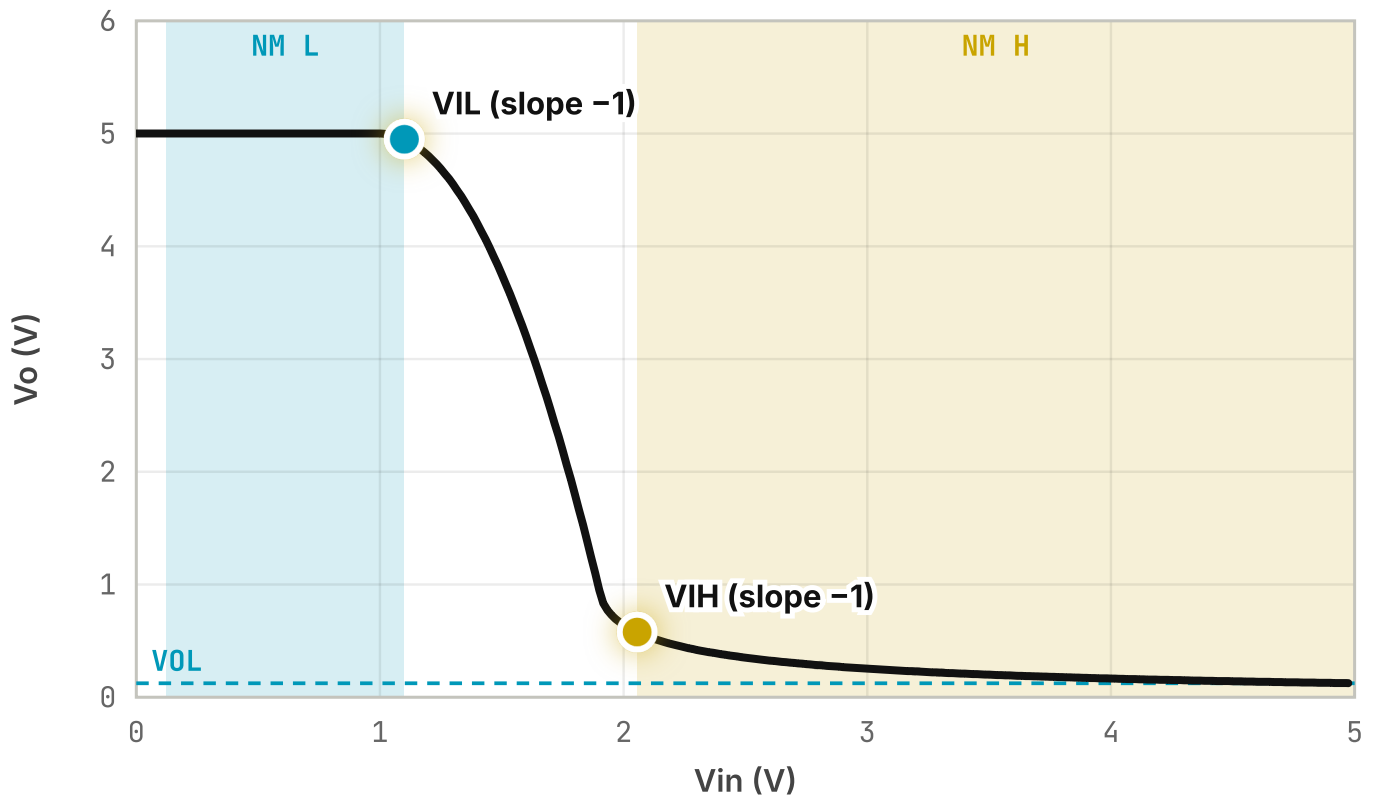
08 CONCEPT 33–37 min

The resistive-load NMOS inverter

- $V_{in} < V_T$: MOSFET off, $V_o = V_{DD} = V_{OH}$.
- Just past V_T : **saturation**, $V_o = V_{DD} - R_D k(V_{in} - V_T)^2$, falling fast.
- V_{in} high: **triode**, $r_{DS(on)} \ll R_D$ gives a small V_{OL} .

The edges of the "valid" input bands are where the curve's **slope is -1**: below V_{IL} and above V_{IH} noise is attenuated, between them it is amplified.

$$NM_L = V_{IL} - V_{OL} \quad NM_H = V_{OH} - V_{IH}$$



$V_{DD} = 5 \text{ V}$, $R_D = 10 \text{ k}\Omega$, $k = 0.5 \text{ mA/V}^2$, $V_T = 1 \text{ V}$: the next worked example.

09 WORKED EXAMPLE 37-41 min

VTC part 1: V_{OH} , V_{OL} and V_{IL}

GIVEN

Resistive-load NMOS inverter: $V_{DD} = 5 \text{ V}$, $R_D = 10 \text{ k}\Omega$, $k = 0.5 \text{ mA/V}^2$, $V_T = 1 \text{ V}$.

FIND

V_{OH} , V_{OL} , V_{IL} , and the static power with the output low.

Method: equate driver and load currents (Taub & Schilling, MOS inverter)

SOLUTION

- V_{OH} :** input low ($< V_T$) $\rightarrow$ MOSFET off, no current in $R_D \rightarrow V_{OH} = V_{DD} = 5 \text{ V}$.
- V_{OL} :** input = $V_{OH} = 5 \text{ V}$. Guess triode, equate currents (mA, $\text{k}\Omega$), take the smaller root:

$$(5 - V_o)/10 = 0.5 [2(4)V_o - V_o^2] \Rightarrow 0.5V_o^2 - 4.1V_o + 0.5 = 0$$

$$V_{OL} = 4.1 - \sqrt{4.1^2 - 1} = 0.124 \text{ V}$$

The other root, 8.08 V, is above V_{DD} : impossible. Check $0.124 \text{ V} < 4 \text{ V}$: triode $\checkmark$

- V_{IL} :** just past V_T the driver is saturated, $V_o = 5 - 5(V_{in} - 1)^2$:

$$\frac{dV_o}{dV_{in}} = -10(V_{in} - 1) = -1 \Rightarrow V_{IL} = 1.1 \text{ V}$$

In general $V_{IL} = V_T + 1/(2kR_D)$. $V_o = 4.95$ V there: saturation ✓.

4. **Static power** (output low): $I = (5 - 0.124)/10 \text{ k}\Omega = 0.488 \text{ mA}$, so $P = 5 \text{ V} \times 0.488 \text{ mA} = \mathbf{2.44 \text{ mW}}$. With the output high, $I = 0$.

ANSWER

$V_{OH} = 5 \text{ V}$, $V_{OL} = 0.124 \text{ V}$, $V_{IL} = 1.1 \text{ V}$, $P_{low} = 2.44 \text{ mW}$.

10 **WORKED EXAMPLE** 41-45 min

VTC part 2: V_{IH} and noise margins

GIVEN

Same inverter ($a = kR_D = 5 \text{ V}^{-1}$). From part 1: $V_{OH} = 5 \text{ V}$, $V_{OL} = 0.124 \text{ V}$, $V_{IL} = 1.1 \text{ V}$.

FIND

V_{IH} , NM_L and NM_H .

Method: slope -1 by implicit differentiation, solved together with the VTC

SOLUTION

1. Driver in triode: $V_o = 5 - 5[2(V_{in} - 1)V_o - V_o^2]$. Differentiate w.r.t. V_{in} and put $dV_o/dV_{in} = -1$:

$$1 = 5 [4V_o - 2(V_{in} - 1)] \Rightarrow V_{in} - 1 = 2V_o - 0.1$$

2. Substitute back into the VTC:

$$V_o = 5 - 15V_o^2 + V_o \Rightarrow V_o = \sqrt{1/3} = 0.577 \text{ V}, \quad V_{IH} = 1 + 2(0.577) - 0.1 = 2.05 \text{ V}$$

Check: $V_{DS} = 0.577 \text{ V} < V_{GS} - V_T = 1.05 \text{ V}$, triode ✓.

3. **Noise margins:**

$$NM_L = 1.1 - 0.124 = 0.98 \text{ V}, \quad NM_H = 5 - 2.05 = 2.95 \text{ V}$$

ANSWER

$V_{IH} = 2.05 \text{ V}$, $NM_L = 0.98 \text{ V}$, $NM_H = 2.95 \text{ V}$. Noise must be almost 3 V to upset a 1, but under 1 V upsets a 0.

Your turn • 1: pick R_D

1 EXAM CQ

Same MOSFET ($k = 0.5 \text{ mA/V}^2$, $V_T = 1 \text{ V}$), $V_{DD} = 5 \text{ V}$, input high = 5 V.

The next stage needs $V_{OL} \leq 0.2 \text{ V}$. Find the **minimum R_D** , pick a standard E12 value, and give the static power when the output is low.

SOLUTION

1. At the limit, $V_o = 0.2 \text{ V} < V_{GS} - V_T = 4 \text{ V} \rightarrow$ triode:

$$I_D = 0.5 [2(4)(0.2) - 0.2^2] = 0.78 \text{ mA}$$

2. R_D must drop the rest of V_{DD} at that current:

$$R_D = \frac{5 - 0.2}{0.78 \text{ mA}} = 6.15 \text{ k}\Omega$$

3. A bigger R_D needs less current, so V_{OL} falls: $R_D \geq 6.15 \text{ k}\Omega$. Next E12 value: 6.8 k Ω . Solving again:

$$V_{OL} = 0.181 \text{ V}, \quad I = 0.709 \text{ mA}, \quad P = 3.54 \text{ mW}$$

ANSWER

$R_{D(\min)} = 6.15 \text{ k}\Omega$; choose 6.8 k $\Omega \rightarrow V_{OL} \approx 0.18 \text{ V}$, $P \approx 3.5 \text{ mW}$. Bigger R_D : better 0, less power, but slower rising edge.

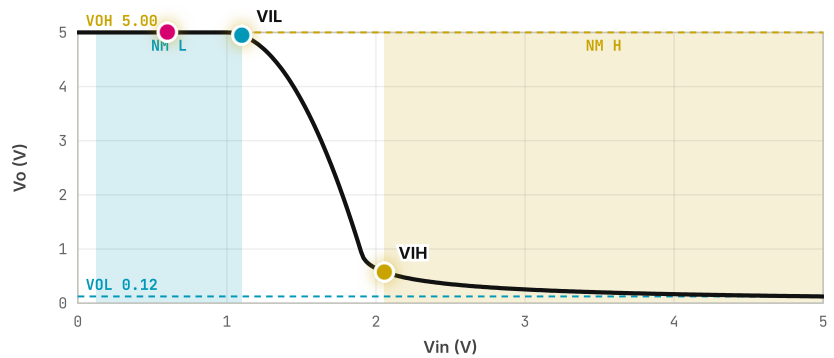
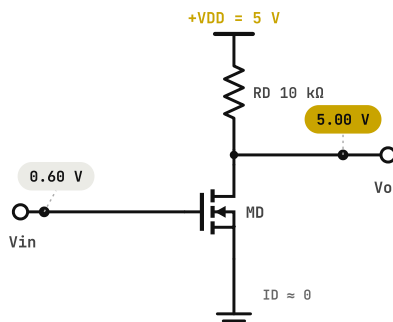
Swap the resistor for a transistor

A 10 k Ω on-chip resistor is huge, and slow: into 1 pF it rises in $2.2R_D C_L = 22 \text{ ns}$, while $r_{DS(on)} = 250 \Omega$ pulls down in $\approx 0.55 \text{ ns}$. Use a **transistor as the load**.

NMOS inverter lab

Pick a load, slide V_{in} , then compare the noise margins and the static power when the output is low.

Resistor R_D from V_{DD} : the textbook starting point.



$V_{in} = 0.60 \text{ V}$ $R_D = 10 \text{ k}\Omega$

V_{OH} / V_{OL}

5.00 / 0.124 V

V_{IL} / V_{IH}

1.10 / 2.05 V

$NM_L = V_{IL} - V_{OL}$

0.98 V

$NM_H = V_{OH} - V_{IH}$

2.95 V

STATIC I (OUT LOW)

488 μA

$P = V_{DD} \cdot I$ (OUT LOW)

2.44 mW

13 **YOUR TURN** 54-58 min

Your turn • 2: the

enhancement-load inverter

2

EXAM CQ

Enhancement-load NMOS inverter: $V_{DD} = 5\text{ V}$, both $V_T = 1\text{ V}$, driver $k_D = 0.5\text{ mA/V}^2$, load $k_L = 0.05\text{ mA/V}^2$. Ignore body effect.

Find (a) V_{OH} , (b) V_{OL} when $V_{in} = V_{OH}$, (c) the static power with the output low.

SOLUTION

1. Load: $V_{GS} = V_{DS} = 5 - V_o \geq V_{GS} - V_T$, so it is always saturated when on. **V_{OH} :** driver off, so I_L must be 0:

$$I_L = k_L(5 - V_o - 1)^2 = 0 \Rightarrow V_{OH} = 4\text{ V}$$

2. **V_{OL} :** $V_{in} = V_{OH} = 4\text{ V}$, driver in triode; equate currents, multiply by 20, take the smaller root (the other is 5.94 V):

$$0.5 [2(3)V_o - V_o^2] = 0.05(4 - V_o)^2 \Rightarrow 11V_o^2 - 68V_o + 16 = 0$$
$$V_{OL} = \frac{68 - \sqrt{3920}}{22} = 0.245\text{ V}$$

3. Static power with the output low:

$$I = 0.05(4 - 0.245)^2 = 0.705\text{ mA}, \quad P = 5(0.705) = 3.52\text{ mW}$$

ANSWER

$V_{OH} = 4\text{ V}$, $V_{OL} = 0.245\text{ V}$, $P_{low} = 3.52\text{ mW}$. It needs $k_D/k_L = 10$ to get a good 0.

14 THINK DEEPER 58-60 min

Critical thinking • the load that gives up early

THINK DEEPER

Why can the enhancement-load inverter **never** output the full 5 V, however long you wait?

The output *is* the load's source. The higher the output climbs, the smaller the load's V_{GS} . At $V_o = V_{DD} - V_T$ the load switches itself off: **$V_{OH} = 4\text{ V}$** , and the last part of the climb is very slow.

A STRONG ANSWER MENTIONS

- The load conducts only while $V_{GS} = V_{DD} - V_o > V_T$.
- As V_o rises toward $V_{DD} - V_T$, the load starves itself and turns off.
- Body effect makes it worse ($\approx 3.5\text{ V}$ in practice); a depletion load ($V_T < 0$) or CMOS pull-up fixes it.

THINK DEEPER

Same inverter, but $k_D = k_L$ (ratio 1). What is V_{OL} ? Why is NMOS called *ratioed* logic?

$V_{OL} = 1.44 \text{ V}$: not a 0 at all. Pull-down and pull-up fight; the output is set by who is stronger. NMOS gates need $k_D/k_L \approx 4\text{--}10+$, costing area.

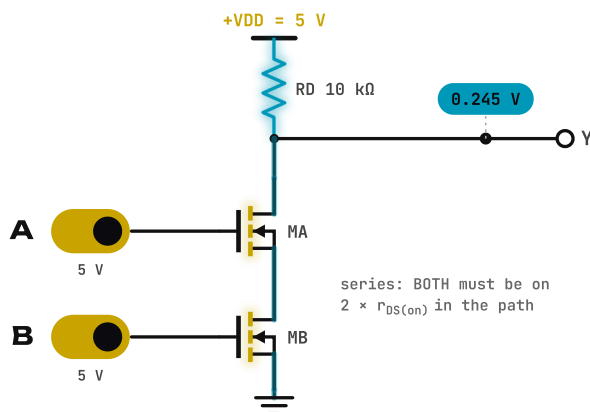
A STRONG ANSWER MENTIONS

- $0.5[6V_o - V_o^2] = 0.5(4 - V_o)^2$ gives $V_o^2 - 7V_o + 8 = 0$.
- $V_{OL} = (7 - \sqrt{17})/2 = 1.44 \text{ V}$: in the forbidden zone.
- A valid 0 exists only if the driver is much stronger than the load: the transistor sizes must be in the right ratio.

15 **LIVE LAB** 60–64 min

NMOS NOR and NAND: parallel or series

NMOS NAND / NOR lab Flip A and B. Current (and power) flows only when a path to ground exists. Compare the '0' of the two gates.



A	B	V_Y	Y	I (mA)
0	0	5.000 V	1	0.000
0	1	5.000 V	1	0.000
1	0	5.000 V	1	0.000
1	1	0.245 V	0	0.475

$R_{DS(ON)}$ EACH

250 Ω

P NOW

2.38 mW

Two in series $\approx 500 \Omega$. $V_{OL} = 0.245 \text{ V}$, double a lone inverter's 0.124 V. Try W/L 2 $\times$.

16 **YOUR TURN** 64–67 min

Your turn • 3: the price

of series transistors

3

EXAM CQ

Two-input NMOS NAND: $R_D = 10 \text{ k}\Omega$, $V_{DD} = 5 \text{ V}$, each pull-down $k = 0.5 \text{ mA/V}^2$, $V_T = 1 \text{ V}$, $A = B = 5 \text{ V}$.

Estimate V_{OL} , compare it with a single inverter, and find the k (W/L) each transistor needs to restore the inverter's V_{OL} .

SOLUTION

1. Each pull-down ($V_{GS} \approx 5 \text{ V}$):

$$r_{DS(on)} = \frac{1}{2(0.5)(5 - 1)} = 0.25 \text{ k}\Omega$$

2. Two in series with R_D :

$$V_{OL} \approx 5 \cdot \frac{0.5}{10 + 0.5} = 0.238 \text{ V}$$

Exact numerical solution: 0.245 V. The upper transistor's V_{GS} is slightly less than 5 V because its source sits above ground.

3. Single inverter for comparison:

$$V_{OL} \approx 5 \cdot \frac{0.25}{10.25} = 0.122 \text{ V} \quad (\text{exact } 0.124 \text{ V})$$

4. Double W/L ($k = 1 \text{ mA/V}^2$): each $r_{DS(on)} = 0.125 \text{ k}\Omega$, stack = 0.25 k Ω , so V_{OL} is back to $\approx 0.122 \text{ V}$.

ANSWER

$V_{OL} \approx 0.24 \text{ V}$, twice the inverter's. Restore it with $k = 1 \text{ mA/V}^2$ ($2 \times$ W/L) per transistor. An n-input NMOS NAND needs $n \times$ W/L on each pull-down.

Critical thinking • NAND or NOR?



TRAP

A classmate's notes say: **"NAND is always preferred over NOR, in every logic family."**

Is that true for NMOS logic? Does your answer change for CMOS? Justify with what you saw in the gate lab.

SOLUTION

1. **NMOS:** NOR puts pull-downs in parallel; each can be minimum size, and V_{OL} never gets worse than an inverter's.
2. NMOS NAND stacks them in series; an n -input NAND needs $n \times W/L$ per transistor, and a taller stack also discharges the load more slowly.
3. So in **NMOS, NOR is preferred** (NMOS-era PLAs were NOR–NOR arrays).
4. **CMOS (next week):** NAND has series NMOS + parallel PMOS; NOR has series PMOS. Holes are 2–3 $\times$ slower than electrons, so series PMOS are costly: in **CMOS, NAND is preferred**.

ANSWER

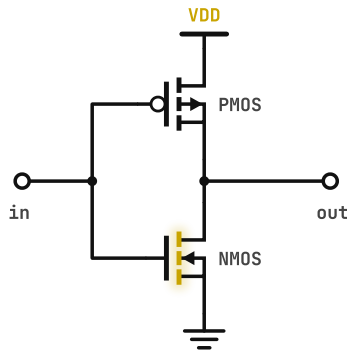
The claim is false for NMOS: NOR wins there. It is true for CMOS, because the series devices in a CMOS NAND are the faster NMOS.

The NMOS power tax, and the CMOS escape

Every NMOS gate with its output low draws $P = V_{DD} \cdot I$ continuously. Our inverter: 2.44 mW.

One million such gates, half of them low: $1 \times 10^6 \times 0.5 \times 2.44 \text{ mW} \approx 1.2 \text{ kW}$. This is why NMOS chips of the late 1970s ran warm with only tens of thousands of transistors.

CMOS pairs a PMOS pull-up with an NMOS pull-down on the same input. In either steady state one of them is *off*, so there is no path from V_{DD} to ground: static current $\approx$ leakage only, $V_{OH} = V_{DD}$, $V_{OL} = 0$.



PRO TIP

Try the **CMOS** tab in the inverter lab: full 0–5 V swing, a symmetric VTC, and static power ≈ 0 . Power is now spent only while *switching*. Next week: CMOS in depth, plus TTL, ECL and I²L.

19 **REAL WORLD** 72–75 min

A MOSFET that makes a battery last a month

A finger pulse oximeter or an ECG patch has an analog front end and LEDs that draw a few mA. A **MOSFET load switch** between the battery and that circuitry turns it on only while measuring: *power gating*.

220 MAH CELL	AVERAGE CURRENT	BATTERY LIFE
Front end always on (3 mA)	3 mA	≈ 73 h (3 days)
Gated: on 10 % + 5 μ A sleep	0.305 mA	≈ 721 h (30 days)

A switch with $r_{DS(on)} = 50 \text{ m}\Omega$ drops only $3 \text{ mA} \times 50 \text{ m}\Omega = 0.15 \text{ mV}$: the sensor never notices it is there.



BME CORNER

For a community health worker screening children for pneumonia (low SpO_2) in a rural upazila, a device that runs a month between charges is the difference between used and abandoned. Every wearable ECG and glucose monitor uses the same trick.



DRONE CORNER

A quadcopter, like the student-built drones flown at Bangladeshi university robotics fests, spins each motor with an ESC: an H-bridge (or 3-phase bridge) of power MOSFETs at tens of kHz, each with a gate driver, exactly the design from slide 7.

20 **POP QUIZ** 75–78 min

Pop quiz

1. An NMOS has $V_T = 1\text{ V}$, $V_{GS} = 3\text{ V}$ and $V_{DS} = 1\text{ V}$. It is in...

A. Cutoff

B. Triode (ohmic) ✓

C. Saturation

D. Breakdown

Overdrive $V_{GS} - V_T = 2\text{ V}$. $V_{DS} = 1\text{ V}$ is below it, so the channel is not pinched off: triode.

2. $k = 0.5\text{ mA/V}^2$, $V_T = 1\text{ V}$, $V_{GS} = 3\text{ V}$, $V_{DS} = 5\text{ V}$. $I_D = ?$

A. 1 mA

B. 2 mA ✓

C. 4 mA

D. 4.5 mA

$V_{DS} \geq 2\text{ V} \rightarrow$ saturation: $I_D = 0.5 \times 2^2 = 2\text{ mA}$.

3. A MOSFET in *saturation* behaves most like a BJT in...

A. Saturation (closed switch)

B. Cutoff

C. The active region (current source) ✓

D. Reverse active

Name trap. MOSFET saturation = current saturates = a current source, like BJT active. The closed-switch MOSFET region is triode.

4. Enhancement-load NMOS inverter, $V_{DD} = 5\text{ V}$, $V_T = 1\text{ V}$ (ignore body effect). $V_{OH} = ?$

A. 5 V

B. 4.3 V

C. 4 V ✓

D. 3 V

The load (gate = drain = V_{DD}) turns off when $V_{GS} = V_{DD} - V_o$ falls to V_T : $V_{OH} = 5 - 1 = 4\text{ V}$.

5. An NMOS resistive-load gate draws static power when its output is...

A. High

B. Low ✓

C. Switching only

D. Never

Output low means a pull-down path conducts from V_{DD} to ground: $P = V_{DD} \cdot I$ all the time the output stays low. CMOS removes this path.

21 **RECAP** 78-80 min

Three things to remember

01

$V_{GS} > V_T$ builds the channel. **Triode** ($V_{DS} < V_{GS} - V_T$) is the closed switch, $r_{DS(on)} \approx 1/[2k(V_{GS} - V_T)]$. Saturation is a current source.

02

NMOS inverter: V_{IL} , V_{IH} at slope -1 ; $NM_L = V_{IL} - V_{OL}$, $NM_H = V_{OH} - V_{IH}$. Enhancement load: $V_{OH} = V_{DD} - V_T$, ratioed.

03

NOR = parallel, NAND = series (needs $n \times W/L$). Output low = static power $V_{DD} \cdot I$. CMOS removes it: next week.

HW

BEFORE NEXT CLASS

A 3.3 V resistive-load NMOS inverter: $R_D = 20 \text{ k}\Omega$, $k = 0.25 \text{ mA/V}^2$, $V_T = 0.7 \text{ V}$. Find V_{OL} , V_{IL} , V_{IH} , both noise margins and the static power with the output low. Check each region.

SOLUTION

1. $kR_D = 0.25 \times 20 = 5 \text{ V}^{-1}$. $V_{OH} = 3.3 \text{ V}$. V_{OL} (triode, $V_{in} = 3.3 \text{ V}$):

$$\frac{3.3 - V_o}{20} = 0.25 [5.2V_o - V_o^2] \Rightarrow V_{OL} = 0.125 \text{ V}$$

2. V_{IL} (driver saturated): $V_{IL} = V_T + 1/(2kR_D) = 0.7 + 0.1 = \mathbf{0.80 \text{ V}}$.

3. V_{IH} (driver triode), using the closed form from the worked example:

$$V_o = \sqrt{3.3/15} = 0.469 \text{ V}, \quad V_{IH} = 0.7 + 2(0.469) - 0.1 = 1.54 \text{ V}$$

4. Margins and power:

$$NM_L = 0.68 \text{ V}, \quad NM_H = 1.76 \text{ V}, \quad P_{low} = 3.3 \cdot \frac{3.3 - 0.125}{20} = 0.52 \text{ mW}$$

ANSWER

$V_{OL} \ 0.125 \text{ V} \cdot V_{IL} \ 0.80 \text{ V} \cdot V_{IH} \ 1.54 \text{ V} \cdot NM_L \ 0.68 \text{ V} \cdot NM_H \ 1.76 \text{ V} \cdot P_{low} \ 0.52 \text{ mW}$

S. M. Sakeef Sani

Adjunct Lecturer, CSE · Northern University Bangladesh

smsakeefsani.hbitcorp.com