

TTL: inside the 7400

Four transistors, four resistors and a diode: the gate that ran digital electronics for twenty years, and still sets the voltage levels your Arduino talks in.

01 COLD OPEN 0–4 min

A video game with no processor

Atari's **Pong** (1972) had no CPU and no software. The whole game was a board of a few dozen **7400-series TTL** chips: counters, gates and flip-flops.

The same chips built minicomputers, cash registers and early medical monitors. Their voltage levels (0.8 V and 2.0 V) are still printed on Arduino and ESP32 datasheets as “TTL-compatible”.

THINK DEEPER

Last week's DTL gate was slow when its output went from 0 to 1. Why? (Hint: what pulls the output up?)

The rising edge is an **RC charge** through a resistor of a few k Ω . Pulling down is done by a saturated transistor (fast); pulling up is done by a resistor (slow). TTL puts a transistor on *both* sides.

A STRONG ANSWER MENTIONS

- The pull-up is a passive collector resistor R_C (k Ω).
- It must charge the load and wiring capacitance: $\tau = R_C C_L$, tens of ns.
- TTL replaces it with an active transistor pull-up: the totem pole.

02 CONCEPT 4–8 min

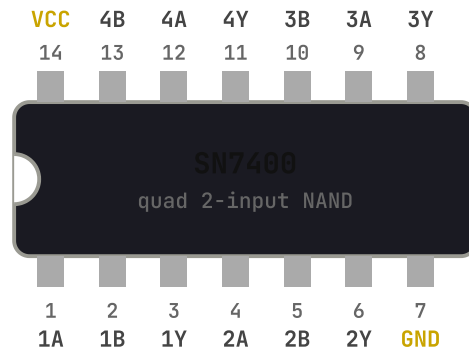
From DTL to TTL in two moves

- 1 **Input diodes** → **one multi-emitter transistor Q1**. Each emitter is an input. When all inputs go high, Q1 runs “backwards” and drives Q2. When an input goes low, Q1 *actively pulls* the stored charge out of Q2's base: faster turn-off.

2 Collector resistor → totem-pole output. Q3 (pull-up, an emitter follower) and Q4 (pull-down) stacked between V_{CC} and ground. Q2, the *phase splitter*, turns exactly one of them on.

PRO TIP

The name: the **input** is a transistor (not a diode), and so is the output, hence **Transistor-Transistor Logic**.



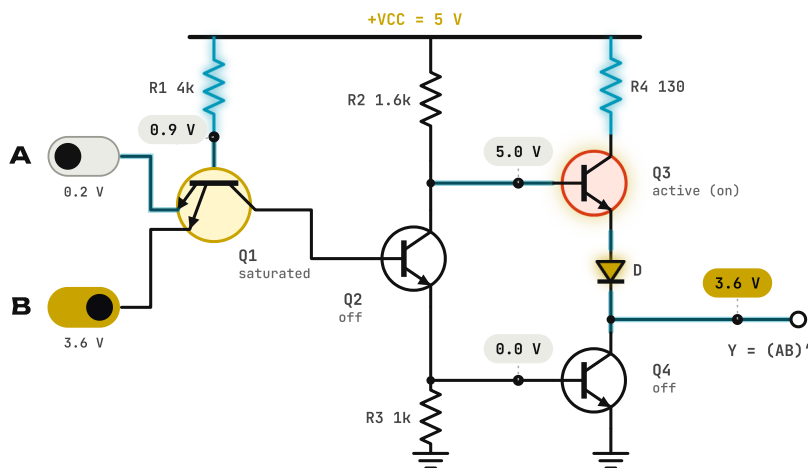
Pin 14 = +5 V, pin 7 = ground: the corners, on every 14-pin 74-series chip. Each gate: $Y = (AB)'$.

03 LIVE LAB 8-15 min

Live lab: follow the current through a 7400 gate

Inside the 7400: one TTL NAND gate

Flip A and B. Follow the current, read the node voltages, then pull out the diode or overload the output.



OUTPUT **1 (HIGH)** 0 NAND 1

I_{R1} 1.02 mA out of the low input

I_{R2} ≈ 0 tiny: Q3 base

I_{B4} 0 Q4 off

I_{CC} 1.18 mA $P = 5.9$ mW

✓ diode D fitted

fan-out: **4** TTL inputs on Y

Low: sink 4×1.6 mA = 6.4 of 16 mA

High: source 4×40 μ A = 160 of 400 μ A

04 WORKED EXAMPLE 15-21 min

Worked example 1: an input

LOW, the output HIGH

GIVEN

Standard TTL NAND (7400): $R_1 = 4\text{ k}\Omega$, $R_2 = 1.6\text{ k}\Omega$, $R_3 = 1\text{ k}\Omega$, $R_4 = 130\text{ }\Omega$, $V_{CC} = 5\text{ V}$. $V_{BE(\text{on})} = 0.7\text{ V}$, $V_{CE(\text{sat})} = 0.2\text{ V}$, $V_D = 0.7\text{ V}$. Input A = 0.2 V, B = 3.6 V.

FIND

V_{B1} , the input current, the state of each transistor, V_{OH} and the supply power.

Method: assume transistor states, compute, then check (Millman & Taub, Taub & Schilling TTL analysis)

SOLUTION

1. Input A = 0.2 V (a low from another TTL gate). Q1's A-emitter junction conducts, so the base sits one V_{BE} above it:

$$V_{B1} = 0.2 + 0.7 = 0.9\text{ V}$$

2. Current through R_1 , which leaves through the A pin into the gate that drives it:

$$I_{R1} = \frac{5 - 0.9}{4\text{ k}\Omega} = 1.025\text{ mA} \quad (\text{datasheet worst case } I_{IL} = 1.6\text{ mA})$$

3. Q1 is saturated, so $V_{B2} \approx 0.2 + 0.1 = 0.3\text{ V}$. Q2 needs about 0.6–0.7 V to conduct: **Q2 off, so Q4 off** (no base current).
4. R_2 now pulls Q3's base towards 5 V; Q3 is an emitter follower driving the output through D:

$$V_{OH} = 5 - V_{BE3} - V_D = 5 - 0.7 - 0.7 = 3.6\text{ V}$$

Q3's small base current through R_2 is neglected. The datasheet only promises $V_{OH} \geq 2.4\text{ V}$ (worst case, full load).

5. Supply current with the output high: only R_1 carries current.

$$I_{CCH} = 1.025\text{ mA}, \quad P_H = 5 \times 1.025 = 5.1\text{ mW}$$

ANSWER

$V_{B1} = 0.9\text{ V}$, 1.025 mA flows out of input A. Q1 saturated, Q2 and Q4 off, Q3 on. $V_{OH} \approx 3.6\text{ V}$. $P_H \approx 5.1\text{ mW}$.

05 WORKED EXAMPLE 21–27 min

Worked example 2: both inputs HIGH, the output LOW

GIVEN

Same gate. $A = B = 3.6 \text{ V}$.

FIND

V_{B1} , I_{B2} , I_{R2} , Q4's base current, V_{OL} , the state of Q3, and the average power.

Method: reverse-active input transistor, saturated phase splitter (Mano, TTL circuit operation)

SOLUTION

1. $A = B = 3.6 \text{ V}$. Q1's emitters are reverse biased; its base-collector junction is forward biased and feeds Q2's base (Q1 is **reverse-active**). Three junctions from B1 to ground:

$$V_{B1} = V_{BC1} + V_{BE2} + V_{BE4} = 3(0.7) = 2.1 \text{ V}$$

2. Base current for Q2:

$$I_{B2} = I_{R1} = \frac{5 - 2.1}{4 \text{ k}\Omega} = 0.725 \text{ mA}$$

The inputs only draw leakage: $I_{IH} \leq 40 \text{ }\mu\text{A}$ on the datasheet.

3. Q2 saturates on top of Q4's V_{BE} : $V_{E2} = 0.7 \text{ V}$, $V_{C2} = 0.7 + 0.2 = 0.9 \text{ V}$.

$$I_{R2} = \frac{5 - 0.9}{1.6 \text{ k}\Omega} = 2.56 \text{ mA}$$

4. Q2's emitter current splits between R3 and Q4's base:

$$I_{B4} = (0.725 + 2.56) - \frac{0.7}{1 \text{ k}\Omega} = 2.59 \text{ mA} \Rightarrow \text{Q4 saturated, } V_{OL} = 0.2 \text{ V}$$

5. Q3: its base is at 0.9 V but it would need $V_{OL} + V_D + V_{BE3} = 0.2 + 0.7 + 0.7 = 1.6 \text{ V}$. **Q3 off.**

6. Supply current with the output low, and the average power:

$$I_{CCL} = 0.725 + 2.56 = 3.29 \text{ mA}, \quad P_L = 16.4 \text{ mW}, \quad P_{avg} = \frac{5.1 + 16.4}{2} \approx 10.8 \text{ mW}$$

The datasheet's typical figure for a standard TTL gate is 10 mW . Our hand analysis lands right on it.

ANSWER

$V_{B1} = 2.1 \text{ V}$, $I_{B2} = 0.725 \text{ mA}$, $I_{R2} = 2.56 \text{ mA}$, $I_{B4} = 2.59 \text{ mA}$, $V_{OL} = 0.2 \text{ V}$, Q3 off. $P_L = 16.4 \text{ mW}$, $P_{avg} \approx 10.8 \text{ mW}$.

Critical thinking · what is the diode for?



TRAP

A student redraws the 7400 output stage and leaves out the diode D “because it just wastes 0.7 V of the output swing”.

Using the node voltages from worked example 2, explain what goes wrong when the output is LOW. What does D cost us?

SOLUTION

1. Output LOW: $V_{\text{out}} = 0.2 \text{ V}$ and Q3's base is at 0.9 V.
2. **Without D**, Q3's emitter sits directly on the output: $V_{\text{BE3}} = 0.9 - 0.2 = 0.7 \text{ V}$. Q3 conducts, and current flows $V_{\text{CC}} \rightarrow R_4 \rightarrow Q3 \rightarrow Q4 \rightarrow \text{ground}$ the whole time the output is low.
3. **With D**, the 0.7 V is shared by two junctions in series (Q3's BE and D), which together need 1.4 V. Neither conducts: Q3 is off.
4. So D removes a static current path and keeps V_{OL} low. The price: V_{OH} is one diode drop lower (3.6 V instead of 4.3 V).

ANSWER

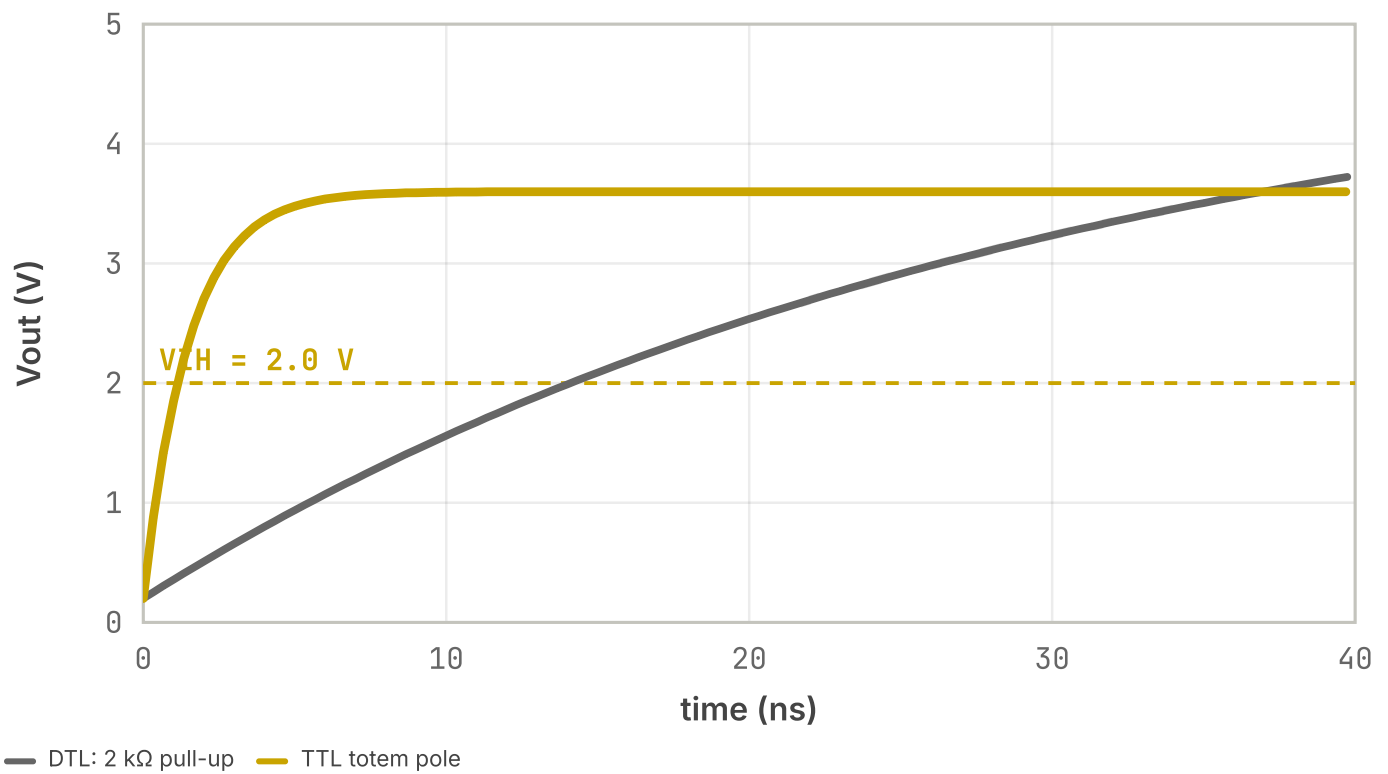
Without D, Q3 would turn on whenever the output is low ($V_{\text{BE3}} = 0.7 \text{ V}$), wasting current through R_4 , Q3 and Q4. D raises the turn-on voltage to 1.4 V so Q3 stays off.

Why the totem pole is fast

Driving 15 pF of load (a few inputs plus wiring) from 0.2 V up to the 2.0 V threshold:

PULL-UP	R ($\approx$)	T = RC_L	TIME TO REACH 2.0 V
DTL resistor	2 k Ω	30 ns	14 ns
TTL totem pole	$\approx 100 \Omega$	1.5 ns	1.1 ns

Q3 as an emitter follower has a low output resistance; with R_4 it is around 100 Ω . Both edges are now driven by a transistor.



08 **YOUR TURN** 34-39 min

Your turn · 1: the 30 mA spike

and the 100 nF capacitor

1

EXAM CQ

- (a) Estimate the current spike through the totem pole while it switches.
- (b) All four gates of a 7400 switch at once; the current rises in 3 ns and the supply wiring has 20 nH of inductance. How big is the dip on V_{CC} ?
- (c) A 100 nF ceramic capacitor is placed across pins 14 and 7. Each spike lasts about 5 ns. Now how big is the dip?

SOLUTION

1. During the transition both totem-pole transistors conduct for a few ns. R_4 alone limits the current:

$$I_{peak} = \frac{5 - V_{CE3(sat)} - V_D - V_{CE4(sat)}}{R_4} = \frac{5 - 0.2 - 0.7 - 0.2}{130 \Omega} = 30 \text{ mA}$$

2. Four gates switching together: 120 mA, rising in 3 ns, through 20 nH of supply wiring:

$$V = L \frac{di}{dt} = 20 \text{ nH} \times \frac{0.12 \text{ A}}{3 \text{ ns}} = 0.8 \text{ V}$$

A 0.8 V dip on V_{CC} (and a bounce on ground) is twice TTL's 0.4 V noise margin: other gates can mis-switch.

3. A 100 nF capacitor right at the chip supplies the spike locally. Charge drawn $\approx 0.12 \text{ A} \times 5 \text{ ns}$:

$$\Delta V = \frac{Q}{C} = \frac{0.6 \text{ nC}}{100 \text{ nF}} = 6 \text{ mV}$$

ANSWER

$I_{peak} \approx 30 \text{ mA}$ per gate. Without decoupling: $\approx 0.8 \text{ V}$ supply dip (more than the noise margin).
With 100 nF at the pins: $\approx 6 \text{ mV}$.

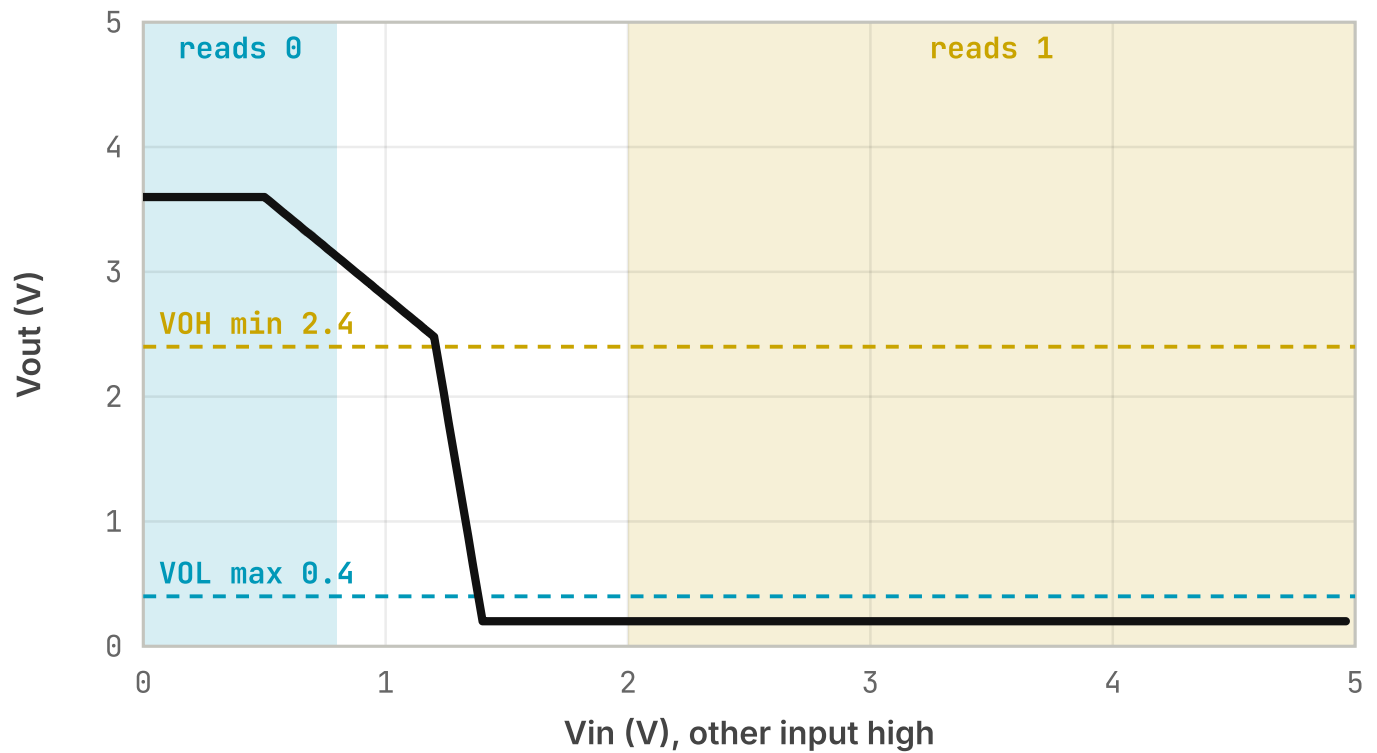
09 CONCEPT 39–43 min

The datasheet view: levels, margins and fan-out

74 SERIES (WORST CASE)	VALUE
$V_{OH(min)} / V_{OL(max)}$	2.4 V / 0.4 V
$V_{IH(min)} / V_{IL(max)}$	2.0 V / 0.8 V
I_{OH} / I_{OL} (output can supply)	0.4 mA / 16 mA
I_{IH} / I_{IL} (each input needs)	40 μA / 1.6 mA

$$NM_H = V_{OH} - V_{IH} = 0.4 \text{ V}, \quad NM_L = V_{IL} - V_{OL} = 0.4 \text{ V}$$

$$\text{fan-out} = \min\left(\frac{I_{OL}}{I_{IL}}, \frac{I_{OH}}{I_{IH}}\right) = \min(10, 10) = 10$$



Typical VTC from our model (switches near 1.3 V). The datasheet limits are guarantees for every chip, at any temperature: much stricter than one typical part.

Your turn • 2: mixing TTL subfamilies

2 EXAM CQ

74LS inputs need $I_{IL} = 0.4 \text{ mA}$ and $I_{IH} = 20 \mu\text{A}$; a 74LS output gives $I_{OL} = 8 \text{ mA}$ and $I_{OH} = 0.4 \text{ mA}$. Standard 74 values are on the previous slide.

(a) How many 74LS inputs can one 7400 output drive? (b) How many standard 7400 inputs can one 74LS00 output drive? Say which state limits each answer.

SOLUTION

1. (a) 7400 driving 74LS inputs, LOW state:

$$\frac{I_{OL}}{I_{IL}} = \frac{16 \text{ mA}}{0.4 \text{ mA}} = 40$$

2. HIGH state:

$$\frac{I_{OH}}{I_{IH}} = \frac{400 \mu\text{A}}{20 \mu\text{A}} = 20 \Rightarrow \text{fan-out} = 20$$

3. (b) 74LS00 driving standard 7400 inputs:

$$\text{LOW: } \frac{8}{1.6} = 5, \quad \text{HIGH: } \frac{400}{40} = 10 \Rightarrow \text{fan-out} = 5$$

4. The low state limits case (b): a 74LS output can sink only 8 mA, and each standard input pushes 1.6 mA into it.

ANSWER

(a) 20 (limited by the HIGH state). (b) 5 (limited by the LOW state).

Schottky TTL: no more saturation

Last week: a saturated BJT stores extra charge in its base and needs a **storage time** t_s to turn off. A **Schottky diode** (metal–semiconductor, $\approx 0.3\text{--}0.4 \text{ V}$) across base–collector diverts the excess base current once V_{CE} drops to about $0.3\text{--}0.4 \text{ V}$. The transistor never saturates deeply: $t_s \approx 0$.

SUBFAMILY	DELAY	POWER / GATE	DELAY × POWER
74 (standard)	9 ns	10 mW	90 pJ
74S (Schottky)	3 ns	20 mW	60 pJ
74LS (low-power Schottky)	9.5 ns	2 mW	19 pJ

SUBFAMILY	DELAY	POWER / GATE	DELAY × POWER
74ALS (advanced LS)	4 ns	1.2 mW	4.8 pJ

PRO TIP

74S kept small resistors and gained speed. 74LS used **larger resistors** (lower current, lower power) and spent the Schottky speed-up on getting back to standard speed: the same 9.5 ns at one fifth of the power.

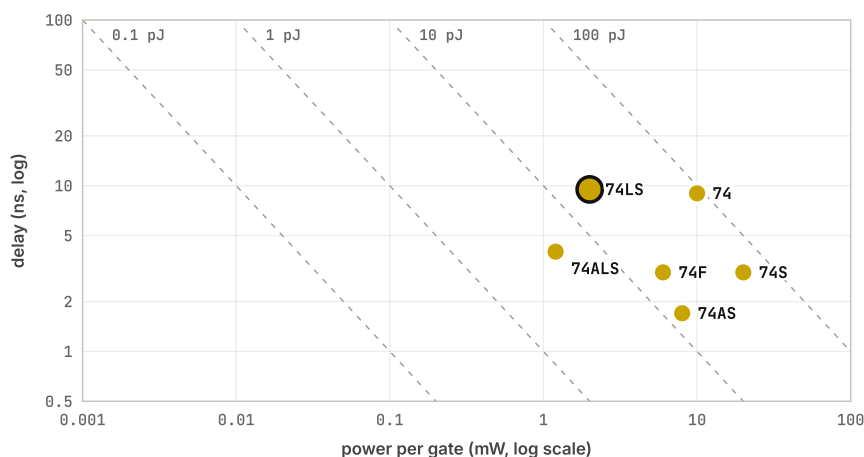
GOTCHA

Speed and power trade against each other. The fair comparison is their product, the **speed–power product** (delay × power, in pJ): the energy per switching event. Lower is better.

12 **LIVE LAB** 51–56 min

Live lab: the TTL family on one chart

TTL subfamilies: speed vs power Lower-left is better: fast and frugal. Dashed lines are equal speed–power products (delay × power, in pJ). Click a family.



● TTL

74LS (LOW-POWER SCHOTTKY)

DELAY
9.5 ns

POWER
2.0 mW

DELAY
×
POWER
19 pJ

Schottky clamps with larger resistors: the workhorse of the 1980s.

Critical thinking • two outputs, one wire



CRITICAL THINKING

To save a gate, a student connects the outputs of two 7400 gates to the same wire, hoping the wire will be HIGH only if both outputs are HIGH (an AND for free).

What happens when one output is HIGH and the other is LOW? Estimate the current. What should they use instead?

SOLUTION

1. Path: $V_{CC} \rightarrow R4 \rightarrow Q3 \rightarrow D$ (gate 1) $\rightarrow$ shared wire $\rightarrow Q4$ (gate 2) $\rightarrow$ ground. Nothing but $R4$ limits it:

$$I \approx \frac{5 - 0.2 - 0.7 - 0.2}{130 \, \Omega} = 30 \, \text{mA, continuously}$$

2. Gate 1's $Q3$ runs at 30 mA (its rated I_{OH} is 0.4 mA); gate 2's $Q4$ sinks 30 mA (rated 16 mA). Both heat up; over time they fail.
3. The wire voltage sits wherever the fight settles: not a guaranteed 0 or 1.
4. Fix: **open-collector** gates (no $Q3$, one shared pull-up resistor) give a safe "wired-AND". Or tri-state outputs. Both in Week 6.

ANSWER

Never tie totem-pole outputs together: when they disagree, ≈ 30 mA flows from V_{CC} through $Q3$ into $Q4$, overheating both, and the logic level is undefined. Use open-collector or tri-state outputs.

Critical thinking • the floating input

THINK DEEPER

A 7400 NAND is used as an inverter; its second input is left **unconnected**. The circuit works on the bench. Why does a floating TTL input act as HIGH, and why is it still a bad idea?

It reads as **HIGH** because current can only flow out of an emitter that has somewhere to go. On a noisy board (motors, relays) the pin picks up glitches and the gate misfires. The datasheet does not guarantee floating inputs, so a good design never relies on them.

A STRONG ANSWER MENTIONS

- No current can leave through an emitter that is connected to nothing, so R1's current goes through Q1's base–collector junction into Q2: the same as a HIGH input.
- But the floating pin is a tiny antenna: noise couples in, and the switching gets slower and unreliable.
- Tie unused inputs to a used input, or to V_{CC} through $\approx 1\text{ k}\Omega$ (the resistor protects the emitter from supply surges).



GOTCHA

Next class: a floating **CMOS** input is far worse. It has no defined level at all and can turn both transistors on at once.

Real world: “TTL serial”, 3.3 V and 5 V

The USB-to-“TTL” serial adapters you use to program an ESP32 or Arduino are named after these levels. Today's chips are CMOS, but they still quote TTL thresholds. Check every connection both ways:

DRIVER → RECEIVER	CHECK	VERDICT
3.3 V CMOS out → 5 V TTL-level in	$V_{OH} \approx 3.2\text{ V} \geq V_{IH} = 2.0\text{ V}$	OK
5 V TTL out → 3.3 V chip in	V_{OH} up to $\approx 3.6\text{ V}$, input max $\approx 3.6\text{ V}$	Risky
5 V CMOS out → 3.3 V chip in	$5\text{ V} > \text{the } 3.6\text{ V input limit}$	Damage: use a level shifter or divider



BME CORNER

A heart-rate or ECG sensor board running at 3.3 V talking to a 5 V microcontroller is a daily lab situation. The threshold arithmetic from today decides whether the data arrives, or the sensor dies.

**DESIGN**

Design a resistor divider so a 5 V output can drive a 3.3 V input safely.

SOLUTION

1. $R1 = 1\text{ k}\Omega$, $R2 = 2\text{ k}\Omega$: $V_{\text{out}} = 5 \times 2/3 = \mathbf{3.33\text{ V}}$: inside the 3.3 V chip's range and well above 2.0 V.

ANSWER

1 k Ω in series, 2 k Ω to ground: 5 V $\rightarrow$ 3.3 V.

16 **POP QUIZ** 68-74 min

Pop quiz

1. **A 7400 input is held LOW by another gate. The current in R1...**

- A. flows into Q2's base
- B. flows out of the input pin into the driving gate ✓**
- C. is zero
- D. flows through Q3

Q1's emitter conducts towards the low input: about 1 mA leaves the pin. That is why a TTL low output must *sink* current, and why I_{OL} sets the fan-out.

2. **The diode D in the totem-pole output exists to...**

- A. protect against reverse supply
- B. keep Q3 off when the output is low ✓**
- C. speed up Q4
- D. raise V_{OH}

With the output low, Q3's base is at 0.9 V. Without D, Q3 would have $V_{BE} = 0.9 - 0.2 = 0.7\text{ V}$ and conduct into Q4. D adds the extra 0.7 V that keeps it off.

3. **Standard TTL: $I_{OL} = 16\text{ mA}$, $I_{IL} = 1.6\text{ mA}$, $I_{OH} = 0.4\text{ mA}$, $I_{IH} = 40\text{ }\mu\text{A}$. Fan-out = ?**

- A. 4
- B. 10 ✓**
- C. 16
- D. 40

$\min(16/1.6, 0.4/0.04) = \min(10, 10) = 10$.

4. **An unused TTL input is left unconnected. The gate treats it as...**

- A. LOW
- B. HIGH ✓**
- C. random
- D. a short circuit

No current can leave the floating emitter, so R1's current goes on into Q2, exactly as for a high input. It works, but it picks up noise: tie it to V_{CC} through 1 k Ω .

5. The "S" in 74LS stands for Schottky. What does the Schottky clamp do?

A. Raises the supply voltage

B. Keeps transistors out of deep saturation, removing storage time ✓

C. Increases fan-out

D. Adds hysteresis

The Schottky diode across base–collector diverts excess base current, so no excess charge is stored: last week's t_s disappears.

17 **RECAP** 74–80 min

Three things to remember

01

Input LOW: $V_{B1} = 0.9\text{ V}$, $\approx 1\text{ mA}$ flows *out* of the input; Q2, Q4 off; Q3 + D give $V_{OH} \approx 3.6\text{ V}$.

Inputs HIGH: $V_{B1} = 2.1\text{ V}$, Q2 and Q4 saturate, $V_{OL} = 0.2\text{ V}$.

02

Totem pole: fast edges both ways, D keeps Q3 off, R4 limits the $\approx 30\text{ mA}$ switching spike (decouple every chip with 100 nF). Never tie totem-pole outputs.

03

Datasheet: $NM = 0.4\text{ V}$, fan-out = $\min(I_{OL}/I_{IL}, I_{OH}/I_{IH}) = 10$. Schottky clamps (74S, 74LS) remove storage time.

HW

BEFORE NEXT CLASS

One 7400 output drives 3 standard TTL inputs and 4 74LS inputs. Check the LOW and HIGH states. How many more 74LS inputs could it drive?

Assignment 1 is published today (logic families), due Week 5, Class 1.

SOLUTION

1. LOW state: $3 \times 1.6 + 4 \times 0.4 = 6.4\text{ mA} \leq 16\text{ mA} \checkmark$. HIGH state: $3 \times 40 + 4 \times 20 = 200\text{ }\mu\text{A} \leq 400\text{ }\mu\text{A} \checkmark$.
2. Spare capacity: LOW $9.6\text{ mA} \div 0.4 = 24$ more; HIGH $200\text{ }\mu\text{A} \div 20 = 10$ more. The HIGH state limits: **10 more** 74LS inputs.

ANSWER

Both states OK. At most 10 more 74LS inputs (limited by the HIGH state).

