

ECL, I²L and CMOS

Three answers to “how do we build a faster, denser, cooler gate?”:
never saturate, never use a resistor, never connect the supply to ground.

01 COLD OPEN 0–4 min

The supercomputer that needed a refrigerator

The **Cray-1** (1976), the fastest computer of its day, ran at 80 MHz. It was built from about 200,000 **ECL** gates and drew around **115 kW**, with Freon cooling pipes running through the frame.

A phone today does thousands of times more work on a few watts, with **CMOS**. Between them sits a third idea, **I²L**, that packed bipolar logic tighter than anything before it.

THINK DEEPER

Why would anyone accept 115 kW of heat for 80 MHz? What was the alternative in 1976?

Because nothing else was fast enough. TTL's saturating transistors took ≈ 10 ns per gate; a few gates per clock cycle and 80 MHz is impossible. ECL's 1–2 ns made it possible, and the price was heat. Today's lecture is about that trade-off, and how CMOS escaped it.

A STRONG ANSWER MENTIONS

- TTL at the time switched in ~ 10 ns per gate: too slow for an 80 MHz pipeline (12.5 ns per clock).
- ECL switched in 1–2 ns, at ≈ 25 mW per gate.
- CMOS existed but was slow (4000-series, ≈ 50 ns): speed won, at any power.

02 CONCEPT 4–8 min

ECL: steer a current, don't switch it

- A **differential pair**: input transistor(s) and a reference transistor at $V_R = -1.3$ V share one emitter resistor R_E , which sets a roughly constant current (≈ 4 mA).
- Input above V_R : the current goes through the input side. Below: through the reference side. A few hundred mV move all of it.

- The collector resistors are small, so the collectors never fall low enough to saturate anything: **no stored charge, no t_s** .
- Emitter followers** buffer both collectors: low output resistance, and you get **OR and NOR** outputs from every gate.

WHY THE ODD SUPPLY?

$V_{CC} = 0$ V (ground) and $V_{EE} = -5.2$ V. The outputs are measured from the ground rail, which is the quietest node on the board. Logic levels: about -0.9 V (1) and -1.75 V (0).



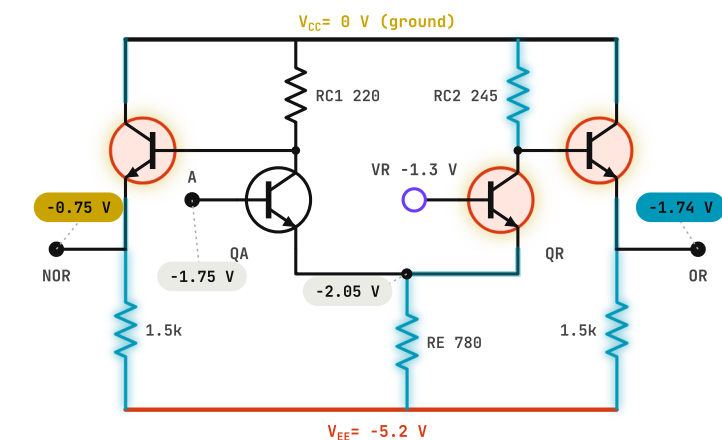
PRO TIP

Extra inputs are just more transistors in parallel with the input transistor: any input above V_R steers the current. So the gate is naturally OR / NOR.

03 **LIVE LAB** 8-14 min

Live lab: watch the current move

ECL: a current switch that never saturates Slide the input past $V_R = -1.3$ V. The same ≈ 4 mA is *steered* from one side to the other; nothing ever saturates.



input A = **-1.75 V** (logic 0 ≈ -1.75 V, logic 1 ≈ -0.75 V)

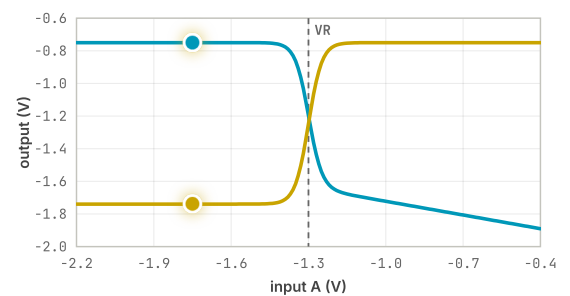
I through QA

I through QR

0.00 mA

4.04 mA

Total stays ≈ 4 mA: the supply sees no spike when the gate switches.



— NOR — OR

QA BASE-COLLECTOR
-1.75 V (reverse)

SWING
 ≈ 1.0 V

04 **WORKED EXAMPLE** 14-20 min

Worked example: an ECL OR/NOR gate

GIVEN

$V_{CC} = 0$, $V_{EE} = -5.2$ V, $V_R = -1.3$ V, $R_E = 780\ \Omega$, $R_{C1} = 220\ \Omega$ (NOR side), $R_{C2} = 245\ \Omega$ (OR side).
 $V_{BE} = 0.75$ V for every conducting transistor (followers included). Neglect base currents.

FIND

I_E , V_{OR} and V_{NOR} for $A = -1.75$ V and for $A = -0.75$ V. Check that the input transistor does not saturate.

Method: find which transistor has the higher base, set V_E from it, then I_E (Millman & Taub, ECL analysis)

SOLUTION

- Inputs LOW ($A = -1.75$ V).** QR has the higher base ($V_R = -1.3$ V), so it conducts and sets the shared emitter node:

$$V_E = V_R - V_{BE} = -1.3 - 0.75 = -2.05\text{ V}, \quad I_E = \frac{-2.05 - (-5.2)}{0.78\text{ k}\Omega} = 4.04\text{ mA}$$

QA: $V_{BE} = -1.75 - (-2.05) = 0.3$ V: off.

- All 4.04 mA flows in QR, through R_{C2} . Each output is a collector seen through a follower (-0.75 V):

$$V_{OR} = -(4.04)(0.245) - 0.75 = -1.74\text{ V (LOW)}, \quad V_{NOR} = 0 - 0.75 = -0.75\text{ V (HIGH)}$$

- Input HIGH ($A = -0.75$ V).** Now QA has the higher base:

$$V_E = -0.75 - 0.75 = -1.5\text{ V}, \quad I_E = \frac{3.7}{0.78} = 4.74\text{ mA}$$

QR: $V_{BE} = -1.3 - (-1.5) = 0.2$ V: off. The current has been *steered*, not switched on and off.

- Outputs swap:

$$V_{NOR} = -(4.74)(0.22) - 0.75 = -1.79\text{ V}, \quad V_{OR} = -0.75\text{ V}$$

- Saturation check** for QA: $V_C = -1.04$ V, $V_B = -0.75$ V, so the base-collector junction has only 0.29 V across it, less than the ≈ 0.5 V it needs to conduct. QA stays **active**: no stored charge, no storage time.

ANSWER

A low: $I_E = 4.04$ mA, OR = -1.74 V, NOR = -0.75 V. A high: $I_E = 4.74$ mA, OR = -0.75 V, NOR = -1.79 V. QA's base-collector is only 0.29 V forward: active, not saturated.

05 **CONCEPT** 20-24 min

ECL: what speed costs

	ECL 10K	74 TTL
Delay	≈ 2 ns	≈ 9 ns

	ECL 10K	74 TTL
Power per gate	≈ 25 mW, constant	≈ 10 mW
Logic swing	≈ 0.85 V	≈ 3.4 V
Noise margins	≈ 0.13 – 0.15 V	0.4 V
Supply current when switching	nearly constant	30 mA spikes
Outputs	OR and NOR, both	one



GOTCHA

Small swing = less charge to move = fast. But small swing also means **small noise margins**. ECL boards need careful layout: $50\ \Omega$ transmission lines, terminations, ground planes.



PRO TIP

Constant current is a hidden advantage: the supply sees no spikes, so ECL generates far less switching noise than TTL.

Your turn • 1: redesign the ECL gate

1 EXAM CQ

The ECL gate is redesigned with $R_E = 1.18 \text{ k}\Omega$ and $R_{C1} = R_{C2} = 300 \Omega$. Everything else as in the worked example ($V_R = -1.3 \text{ V}$, $V_{EE} = -5.2 \text{ V}$, $V_{BE} = 0.75 \text{ V}$).

Find I_E , V_{OR} and V_{NOR} for both input levels, check for saturation, and comment on power and speed.

SOLUTION

1. Input LOW: QR conducts, $V_E = -2.05 \text{ V}$.

$$I_E = \frac{5.2 - 2.05}{1.18} = 2.67 \text{ mA}, \quad V_{OR} = -(2.67)(0.3) - 0.75 = -1.55 \text{ V}, \quad V_{NOR} = -0.75 \text{ V}$$

2. Input HIGH (-0.75 V): QA conducts, $V_E = -1.5 \text{ V}$.

$$I_E = \frac{3.7}{1.18} = 3.14 \text{ mA}, \quad V_{NOR} = -(3.14)(0.3) - 0.75 = -1.69 \text{ V}$$

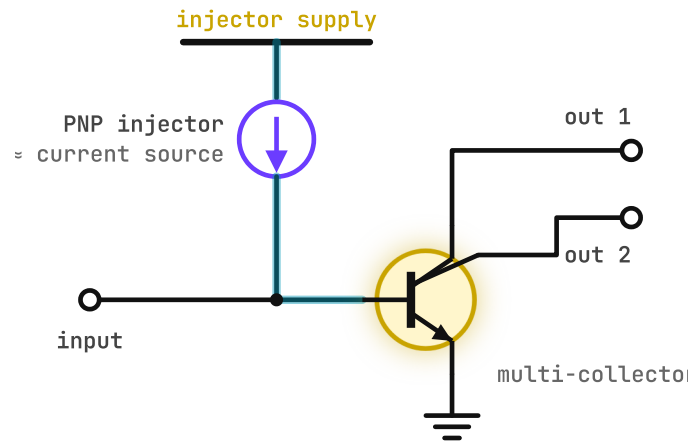
3. Saturation check: $V_C = -0.94 \text{ V}$, $V_B = -0.75 \text{ V} \rightarrow$ base–collector 0.19 V forward: active ✓.
4. Swing ≈ 0.80 – 0.94 V . Less current ($\approx 2.9 \text{ mA}$ average): less power ($\approx 15 \text{ mW}$ instead of $\approx 23 \text{ mW}$), but the larger R_C charges load capacitance more slowly.

ANSWER

Low input: $I_E = 2.67 \text{ mA}$, $OR = -1.55 \text{ V}$, $NOR = -0.75 \text{ V}$. High input: $I_E = 3.14 \text{ mA}$, $NOR = -1.69 \text{ V}$. QA stays active. Lower power, slower edges.

I²L: logic with no resistors at all

- Each gate is one **multi-collector NPN** (run upside down: emitter at ground) fed by a **PNP current injector** that acts as a constant current source into its base.
- Input LOW (another gate pulls the base down): the injector current is diverted, the NPN is **off**, its collectors float (read as 1). Input open: the injector current turns the NPN **on**, collectors pull low (0). It is an inverter.
- No resistors, and the PNP shares regions with the NPN, so a gate takes about the area of **one transistor**. Swing $\approx 0.6 \text{ V}$ (0.1 V to 0.7 V).
- Speed and power are set together by the injector current: double it, and the gate is about twice as fast and uses twice the power (constant speed–power product, $\approx 1 \text{ pJ}$ or less).



POP CULTURE

Texas Instruments built a bipolar version of its TMS9900 microprocessor in I²L (the SBP9900) for harsh-temperature use: I²L packed a whole CPU into bipolar technology.

08 YOUR TURN 32-35 min

Your turn • 2: wiring collectors makes NOR



CRITICAL THINKING

Two I²L inverters have inputs A and B. One collector of each is wired to the same node Y, which feeds the base of the next gate (supplied by its own injector).

Write Y as a function of A and B. How would you make A + B?

SOLUTION

- Gate a's NPN is on when A = 1; gate b's NPN is on when B = 1. Either one ON pulls the shared node Y down.
- Y is HIGH only if both are off: A = 0 **and** B = 0.

$$Y = \bar{A} \cdot \bar{B} = \overline{A + B} \quad (\text{NOR})$$

- The "wired-AND" of inverted signals is a NOR: no extra transistor needed. OR = this NOR followed by one more I²L inverter.

ANSWER

Y = (A + B)': two I²L inverters with their collectors tied form a NOR gate. Add one more inverter for OR.

CMOS: one switch up, one switch down

- A **PMOS** from V_{DD} and an **NMOS** to ground, gates tied together. Input 0: PMOS on, NMOS off, output = V_{DD} . Input 1: the reverse, output = 0 V.
- In either steady state one transistor is **off**: no static current (leakage only), $V_{OH} = V_{DD}$, $V_{OL} = 0$. Full rail-to-rail swing.
- Current flows only while switching: to charge and discharge the load, plus a short "both on" burst near V_M .

$$V_M = \frac{V_{DD} - |V_{Tp}| + V_{Tn}\sqrt{k_n/k_p}}{1 + \sqrt{k_n/k_p}}$$

MATCHED INVERTER ($K_N = K_P$, EQUAL $|V_T|$)

$$V_M = \frac{V_{DD}}{2}$$

$$V_{IL} = \frac{3V_{DD} + 2V_T}{8}, \quad V_{IH} = \frac{5V_{DD} - 2V_T}{8}$$

Noise margins: $NM_L = NM_H = (3V_{DD} + 2V_T)/8$.

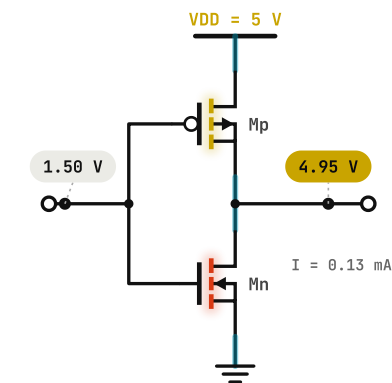


GOTCHA

Electrons are $\approx 2\text{--}3\times$ more mobile than holes. Equal-size transistors are *not* matched: the PMOS must be about $2.5\times$ wider.

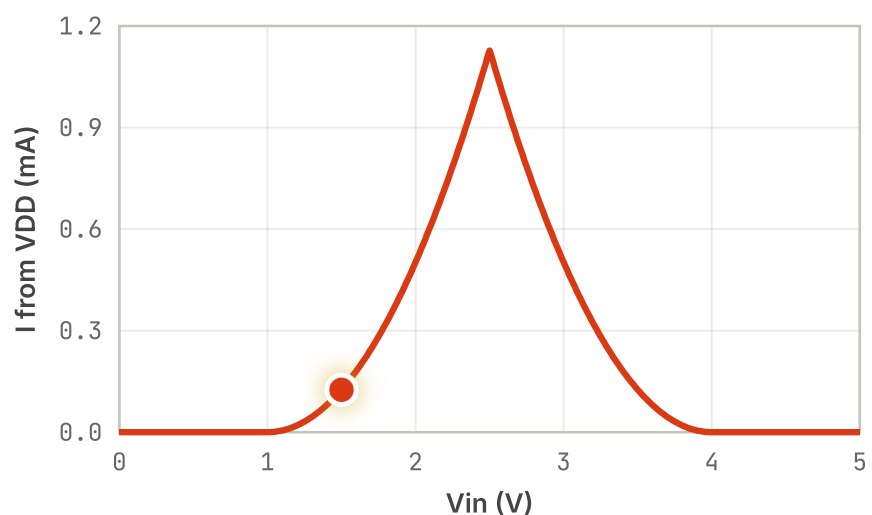
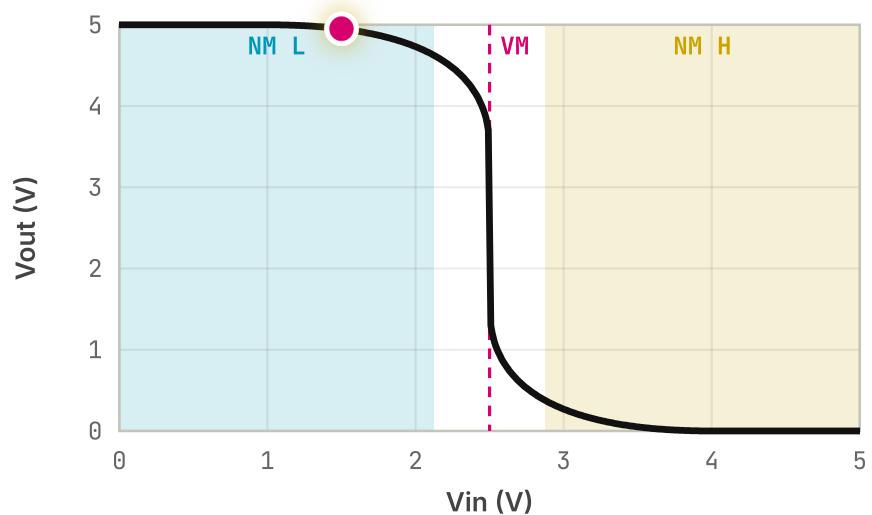
Live lab: the CMOS inverter

CMOS: complementary switches Inverter: slide V_{in} and the n/p strength ratio. Gates: flip A and B and find the path to V_{DD} or to ground. There is never a path through both.



$V_{in} = 1.50 \text{ V}$

$k_n/k_p = 1.00$ (matched)



V_M
2.50 V

V_{IL} / V_{IH}
2.13 / 2.88

NM_L / NM_H
2.13 / 2.13 V

I WHEN IDLE
0

PEAK I AT V_M
1.13 mA

Worked example: the matched CMOS inverter, then the unsized one

GIVEN

CMOS inverter, $V_{DD} = 5\text{ V}$, $V_{Tn} = |V_{Tp}| = 1\text{ V}$, $k_n = k_p = 0.5\text{ mA/V}^2$ (square law, $I_D = k(V_{GS} - V_T)^2$ in saturation).

FIND

V_M , V_{IL} , V_{IH} , both noise margins and the peak supply current. Then V_M if both transistors have the same W/L ($\mu_n = 2.5\mu_p$).

Method: symmetric-inverter formulas (Taub & Schilling, CMOS inverter)

SOLUTION

1. Matched devices ($k_n = k_p$, $V_{Tn} = |V_{Tp}| = V_T$): the VTC is symmetric, so the switching point is mid-supply:

$$V_M = \frac{V_{DD}}{2} = 2.5\text{ V}$$

2. Slope -1 points (derived by equating the two drain currents with NMOS saturated and PMOS triode, and the reverse):

$$V_{IL} = \frac{3V_{DD} + 2V_T}{8} = \frac{15 + 2}{8} = 2.125\text{ V}, \quad V_{IH} = \frac{5V_{DD} - 2V_T}{8} = \frac{25 - 2}{8} = 2.875\text{ V}$$

3. $V_{OH} = 5\text{ V}$ and $V_{OL} = 0\text{ V}$ (no static current, so no drop):

$$NM_L = 2.125 - 0 = 2.125\text{ V}, \quad NM_H = 5 - 2.875 = 2.125\text{ V}$$

Compare TTL: 0.4 V. CMOS margins are about 40 % of V_{DD} .

4. Peak current, at $V_{in} = V_M$, both devices saturated:

$$I_{peak} = k_n(V_M - V_T)^2 = 0.5(1.5)^2 = 1.125\text{ mA}$$

5. Same W/L for both ($\mu_n \approx 2.5\mu_p$, so $k_n/k_p = r = 2.5$):

$$V_M = \frac{V_{DD} - |V_{Tp}| + V_{Tn}\sqrt{r}}{1 + \sqrt{r}} = \frac{5 - 1 + 1.581}{2.581} = 2.16\text{ V}$$

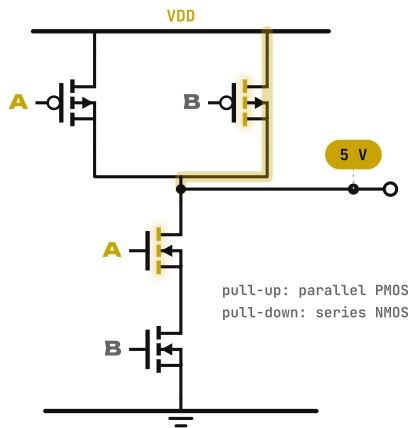
The stronger NMOS drags V_M down. Fix: make the PMOS 2.5× wider, $(W/L)_p = 2.5(W/L)_n$.

ANSWER

$V_M = 2.5\text{ V}$, $V_{IL} = 2.125\text{ V}$, $V_{IH} = 2.875\text{ V}$, $NM_L = NM_H = 2.125\text{ V}$, $I_{peak} = 1.125\text{ mA}$. Equal W/L : $V_M = 2.16\text{ V}$, so widen the PMOS 2.5×.

Live lab: CMOS NAND and NOR

CMOS: complementary switches Inverter: slide V_{in} and the n/p strength ratio. Gates: flip A and B and find the path to V_{DD} or to ground. There is never a path through both.



A	B	PULL-UP	PULL-DOWN	Y
0	0	ON	off	1
0	1	ON	off	1
1	0	ON	off	1
1	1	off	ON	0

In every row exactly one network conducts: the output is always driven, and there is **never a path from V_{DD} to ground**. Static current $\approx$ leakage only.

The networks are *duals*: series in one $\leftrightarrow$ parallel in the other. The NAND's series stack is NMOS (fast electrons): cheap to size up.

CMOS is not free: $P = \alpha C V^2 f$

Every $0 \rightarrow 1$ transition takes energy $C_L V_{DD}^2$ from the supply (half is stored in the load, half burned in the PMOS; the stored half is burned in the NMOS on the way down).

$$P_{dyn} = \alpha C_L V_{DD}^2 f$$

α = activity factor (the fraction of clock cycles in which a node switches), C_L = switched capacitance, f = clock frequency.

ONE 74HC OUTPUT, 50 PF LOAD, $A = 1$	P
5 V, 1 MHz	1.25 mW
3.3 V, 1 MHz	0.54 mW
5 V, 10 MHz	12.5 mW: more than a standard TTL gate



PRO TIP

Three knobs: lower **V** (squared!), lower **f** when idle, switch less (**α** : clock gating). Your phone's processor turns all three every millisecond (dynamic voltage and frequency scaling).

! GOTCHA

At nanometre scales, **leakage** (static current through "off" transistors) is no longer negligible: billions of small leaks. Modern chips power-gate whole blocks off.

14 **YOUR TURN** 57-61 min

Your turn • 3: the power budget of a chip

3 EXAM CQ

A microcontroller switches an effective capacitance of **2 nF** with activity factor **$\alpha = 0.15$** .

(a) Dynamic power at $V_{DD} = 1.8$ V, $f = 100$ MHz? (b) In low-power mode it runs at 1.2 V and 50 MHz. New power? How much of the saving comes from the voltage?

SOLUTION

1. At full speed:

$$P = 0.15 \times 2 \text{ nF} \times (1.8)^2 \times 100 \text{ MHz} = 97.2 \text{ mW}$$

2. Low-power mode:

$$P = 0.15 \times 2 \text{ nF} \times (1.2)^2 \times 50 \text{ MHz} = 21.6 \text{ mW}$$

3. Ratio: $(1.8/1.2)^2 \times (100/50) = 2.25 \times 2 = \mathbf{4.5\times}$ less power. The voltage alone gave 2.25 $\times$.

ANSWER

97.2 mW at full speed, 21.6 mW in low-power mode: 4.5 $\times$ less (2.25 $\times$ from voltage, 2 $\times$ from frequency).

15 **THINK DEEPER** 61-64 min

Critical thinking • never

let a CMOS input float

THINK DEEPER

Last class a floating TTL input read as HIGH. What happens to a floating CMOS input, and why is it worse?

A CMOS input has no current path at all, so nothing decides its level. It wanders to the middle, where **both transistors conduct**: wasted current, heat, and an output that may chatter. Unlike TTL, there is no default.

A STRONG ANSWER MENTIONS

- The gate is a tiny capacitor with no DC path: its voltage drifts with leakage and nearby fields, often to somewhere near V_M .
- Near V_M both transistors are partly on: a steady current flows (the peak in the lab, ≈ 1 mA here) and the output may oscillate.
- Tie every unused CMOS input to V_{DD} or ground (or to a used input). Also: the thin gate oxide is damaged by static (ESD): handle CMOS chips by the edges, store them in conductive foam.



GOTCHA

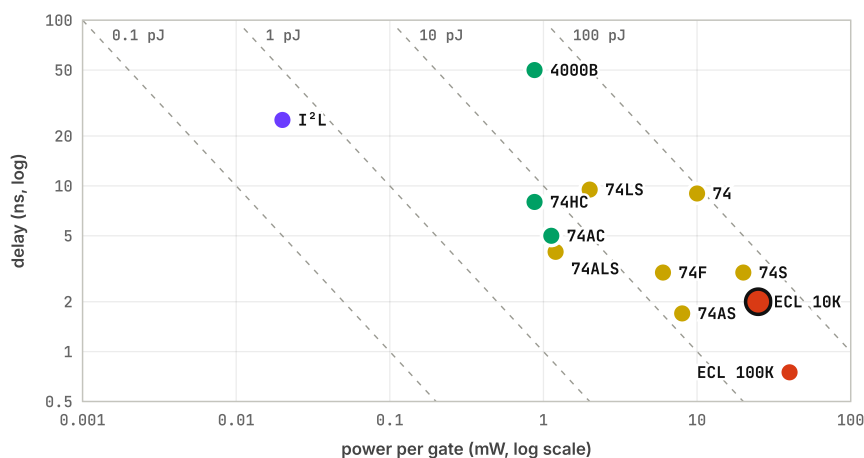
Latch-up: the n and p regions of a CMOS chip form a parasitic thyristor (PNPN). A voltage spike on a pin can trigger it into a short from V_{DD} to ground that only power-cycling clears. Keep input voltages within the supply rails.

16 LIVE LAB 64-68 min

Live lab: every family on one chart

Logic families: speed vs power

Lower-left is better: fast and frugal. Dashed lines are equal speed-power products (delay $\times$ power). Click a family.



● TTL ● ECL ● I²L ● CMOS

ECL 10K

DELAY

2 ns

POWER

25.0 mW

DELAY

$\times$

POWER

50 pJ

Non-saturating current switch,
-5.2 V supply, 0.85 V swing,
NM $\approx$ 0.15 V.

CMOS switching at 1 MHz

CMOS power = $(C_{pd} + 15 \text{ pF}) \cdot V^2 \cdot f$:
slide the frequency and watch only
the CMOS dots move.

Real world: ten years on one battery

An implanted **cardiac pacemaker** senses every heartbeat and fires when one is missed, for 8–10 years on a single lithium battery that cannot be recharged.

$$\frac{1.2 \text{ Ah}}{8 \text{ years} \times 8760 \text{ h/year}} \approx 17 \mu\text{A average, for everything}$$

Sensing amplifiers, the timing logic and the pacing pulses all fit inside about 17 μA . Only CMOS, mostly idle and clocked slowly at a low voltage, can do that. Built from standard TTL, the logic alone would need milliamps: the battery would last days.



BME CORNER

The same logic applies to hearing aids, continuous glucose monitors and capsule endoscopes. In implant design the question is never “how fast?” but “how many joules per decision?”: the speed–power product from today’s chart.

THINK DEEPER

Why is a pacemaker's clock often only tens of kHz, when the chip could run at MHz?

The heart is slow. Running the logic 100× faster would cost 100× the dynamic power and add nothing to the patient.

A STRONG ANSWER MENTIONS

- $P = \alpha CV^2f$: power scales with f .
- A heartbeat comes about once a second; deciding faster gains nothing.
- Lower f also allows lower V , for a V^2 saving on top.

Pop quiz

1. The main reason ECL is faster than TTL is that its transistors...

- A. use a negative supply
- B. never saturate, so there is no storage time ✓**
- C. have more emitters
- D. draw no current

ECL steers a constant current between two transistors that both stay active. Small swing (≈ 0.8 –1 V) and emitter–follower outputs help too.

2. An ECL gate has $V_R = -1.3$ V. Input A = -0.8 V. Which output is HIGH?

A. OR ✓

B. NOR

C. both

D. neither

$A > V_R$, so QA takes the current, its collector (the NOR side) drops, and the reference side's collector rises: OR = HIGH.

3. A CMOS inverter sits at a steady 0 or 1. Its supply current is...

A. about 1 mA

B. set by R_D

C. leakage only, essentially zero ✓

D. largest when the output is low

In either state one transistor is off, so there is no path from V_{DD} to ground. Current flows only while switching.

4. A CMOS chip's supply is lowered from 3.3 V to 1.65 V at the same clock. Dynamic power falls by...

A. 2×

B. 4× ✓

C. 8×

D. not at all

$P = \alpha CV^2f$: halving V divides P by 4. That is why phone processors drop their voltage when idle.

5. In a 2-input CMOS NAND gate the NMOS transistors are...

A. in parallel

B. in series ✓

C. not used

D. one series, one parallel

Output low only if A AND B are 1: both NMOS must conduct, so they are in series. The PMOS (pull-up) network is the dual: parallel.

19 RECAP 77–80 min

Three things to remember

01

ECL steers a constant current ($V_R = -1.3$ V): no saturation, ≈ 1 –2 ns, OR + NOR outputs, but ≈ 25 mW constant and ≈ 0.15 V margins.

02

I²L: injector current source + multi-collector NPN, no resistors, densest bipolar logic; wired collectors give NOR.

O3

CMOS: no static current, rail-to-rail, $NM \approx (3V_{DD} + 2V_T)/8$ when matched (PMOS $\approx 2.5\times$ wider).
Power = αCV^2f .

HW

BEFORE NEXT CLASS

A matched CMOS inverter runs from $V_{DD} = 3.3$ V with $V_T = 0.7$ V. Find V_M , V_{IL} , V_{IH} and the noise margins. It drives 30 pF and toggles every cycle at 20 MHz: dynamic power?

Assignment 1 covers this week (TTL, ECL, I²L, CMOS): due Week 5, Class 1.

SOLUTION

1. Matched: $V_M = 3.3/2 = \mathbf{1.65\text{ V}}$.

$$V_{IL} = \frac{3(3.3) + 2(0.7)}{8} = 1.41\text{ V}, \quad V_{IH} = \frac{5(3.3) - 2(0.7)}{8} = 1.89\text{ V}$$

2. $NM_L = NM_H = \mathbf{1.41\text{ V}}$.

3. Dynamic power:

$$P = 30\text{ pF} \times (3.3)^2 \times 20\text{ MHz} = 6.5\text{ mW}$$

ANSWER

V_M 1.65 V, V_{IL} 1.41 V, V_{IH} 1.89 V, both margins 1.41 V, $P \approx 6.5\text{ mW}$.

S. M. Sakeef Sani

Adjunct Lecturer, CSE · Northern University Bangladesh

smsakeefsani.hbitcorp.com